Photodiode Barrier Induced Lag Characterization Using a New Lag versus Idle Time Methodology

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Abstract

We have developed a new lag versus idle time methodology to identify lag induced by a barrier in the bulk of the Photodiode (PD) region. This method can be easily implemented with conventional pulsed LED lag measurements by inserting idle (non-integration) time before the PD reset to start the integration phase. This new methodology can be used to differentiate and quantify both PD and TX barrier induced lag.

Introduction

BSI and stacking technology in CMOS image sensors (CIS) has enabled more aggressive reduction in pixel size. Many challenges are encountered in developing sub-μm pixel sensors. One of the key challenges is to achieve a high full well capacity (FWC) without introducing image lag. This requires deep PDs where care must be taken to provide a potential profile for fast and complete charge transfer.

Prior work on lag characterization was focused primarily on lag due to the PD to transfer gate (TX) region (edge barrier), [1-4]. With sub-μm high FWC small pixels, incomplete charge transfer can be caused by a potential barrier or well inside the PD, in addition to those at the edge between PD and TX, or between TX and the floating diffusion (FD). This is shown in Figure 1. Edge barrier induced lag can be significantly reduced by increasing the TX_on and FD voltages, while PD barrier induced lag is not sensitive to TX and FD voltages.

Accurate TCAD simulation is needed to design high performance sub-μm pixels. Accurate barrier characterization is required to calibrate the modelled lag barriers. To the authors' knowledge, no method has been reported to identify and characterize a barrier inside of the PD. Here, we are proposing a new lag vs. idle time method to determine if lag is due to a PD barrier, a TX barrier or both, and the amount of lag signal attributed to each one.

Lag vs Idle Time Methodology

Pulsed LED CIS lag measurement is typically done by setting the integration time equal to the frame time ($T_{int} = T_{frame\_line\_length}$). The LED is pulsed on during the vertical blanking time, as shown in Figure 2a. With this operation, pixels from all rows are integrating during the entire LED pulse. Three sets of images, (N dark + N light + N dark frames) are captured. The charging lag is the difference between the last light frame and the first light frame. The discharging lag is the difference between the first dark frame and the last dark frame in the third image set.

With our new lag measurement method, an idle (non-integration) time is inserted by setting $T_{int} < T_{frame\_line\_length}$. In this case, pixels will stay in idle phase before they enter into integration phase. The integration phase is initiated by a TX pulse and RG pulse (shutter operation), as shown in Figure 2b. The region of interest used was limited to the rows that are integrating for the entire LED pulse. Alternately, the LED pulse time can be reduced so that all rows are integrating during the entire LED pulse. As shown in Fig. 3, if the lag is induced by an internal PD barrier, the charge held back by the barrier can emit to the PD region beyond the barrier by thermionic emission during the idle time. The emitted charge can then be transferred and cleared by the shutter operation. If the idle time is longer, the charge emitted over the internal PD barrier increases, and as a result the measured lag decreases as idle time increases. The lag versus idle time should then follow:

$$N(t_{idle}) = N(0) - C_{pd'}[a*\ln(b*t_{idle} + c)]/q + N(TX) \quad \textit{for } t_{idle} \leq \tau_d \text{ ; and } N(t_{idle}) = N(TX); \quad \textit{for } t_{idle} > \tau_d \quad (1)$$

where $C_{pd'}$ = capacitance of the internal PD region that holds charge, $a = 1/\beta$, $\beta = q/mkT$ (the non-ideality factor), $b = I_o\beta/C_{pd'}$, and $c = e^{\beta V(0)}$ [1]. N(TX) is the lag due to a TX barrier as discussed above.

The measured data matches (1) well as shown in Fig. 4. The idle time where the lag flattens out is equal to the PD barrier discharge time (τ_d) [1]. τ_d is given by:

$$\tau_d = [e^{\beta\phi b} - e^{\beta V(0)}]C_{pd'}/\beta I_0 \qquad (2)$$

where ϕb is the internal PD barrier height, and V(0) is the initial potential level with respect to the top of the barrier, (which is zero volts for the LED light level used in our measurements).

By making estimates of $C_{pd'}$ and I_o, ϕb can be calculated from the lag vs. idle time measurement from:

$$\phi b = \ln[(\tau_d\beta I_o/C_{pd'}) + e^{\beta V(0)}]/\beta \qquad (3)$$

Referring to Fig. 5, analysis of the lag vs. idle time curve can determine: (a) if the observed lag is due to a PD barrier, a TX barrier or both; (b) how much of the lag is caused by PD and TX barriers, and (c) the PD barrier discharge time. If the lag is induced by only a TX edge barrier, there is no separate region where the charge can emit to. As a result, the lag vs. idle time is constant.

Experiment and Data Analysis

Various 1.0μm pixel designs with different process conditions were characterized using the lag vs. idle time method. Many pixel designs show zero lag vs idle time, (lag free). Some pixel layouts exhibit both PD and TX barrier induced lag (see Fig. 6a). The lag decreases as idle time increases due to thermionic emission over the PD barrier. When idle time increases to a value where emission ceases (τ_d), lag stays at a constant non-zero value. This is the lag due to a TX barrier, and this level can be reduced by increasing the TX-on voltage as shown. The PD barrier in this design is estimated to be on the order of 0.16 V to 0.22 V.

Other pixel layouts exhibit PD barrier induced lag, but have no TX barrier, (Fig. 6b). Lag goes to zero with increased idle time. Lag vs. idle time does not change with increased TX-on voltage.

Other pixel layouts exhibit TX barrier induced lag, but have no PD barrier, (Fig. 6c). Lag is constant versus idle time. The lag is reduced to zero by increasing TX potential during charge transfer.

Two different pixel layouts with only a PD barrier are shown in Fig. 6d. The two designs have different PD barrier heights, (~0.26 V and ~0.24 V).

The measurement results trends based on design and process variation were used to calibrate TCAD models.

Conclusions

A new lag versus idle time methodology has been developed and demonstrated. This method separates internal PD induced lag from PD to TX induced lag. These results provide more detailed insight into the pixel electrostatic potentials to aid in more accurate calibration of TCAD simulations to facilitate sub-μm pixel design.

References:

[1] Fossum E. R.,Charge transfer noise and lag in CMOS active pixel sensors. IEEE Workshop on CCDs and Advanced Image Sensors, 2003

[2] S. Ramaswami *et al*., Characterization of Pixel Response Time and Image Lag in CMOS Sensors. IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors, 2001.

[3] L. Bonjour *et al*., Experimental Analysis of Lag Sources in Pinned Photodiodes, IEEE Electron Device Letters, Vol. 33,

[4] C. Chen *et al*., Measurement of Charge Transfer Potential Barrier in Pinned Photodiode CMOS Image Sensors, J. of Semiconductor, Vol. 37, No. 5, May 2016

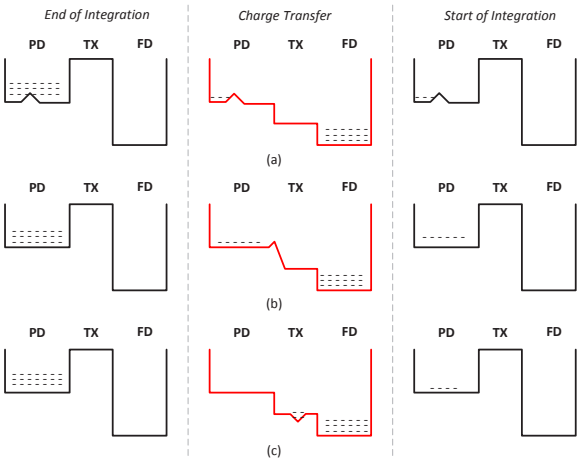


Figure 1. Lag Barrier (or well) locations: (a) barrier inside PD (b) barrier at TX edge (c) well between TX and FD

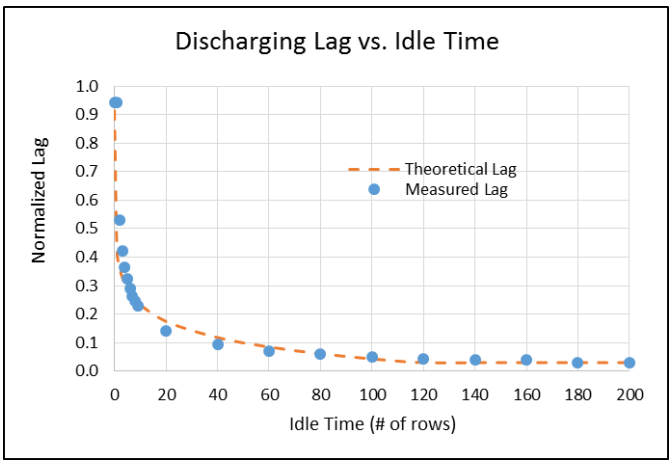


Figure 4. Lag vs. idle time; measured compared to modeled

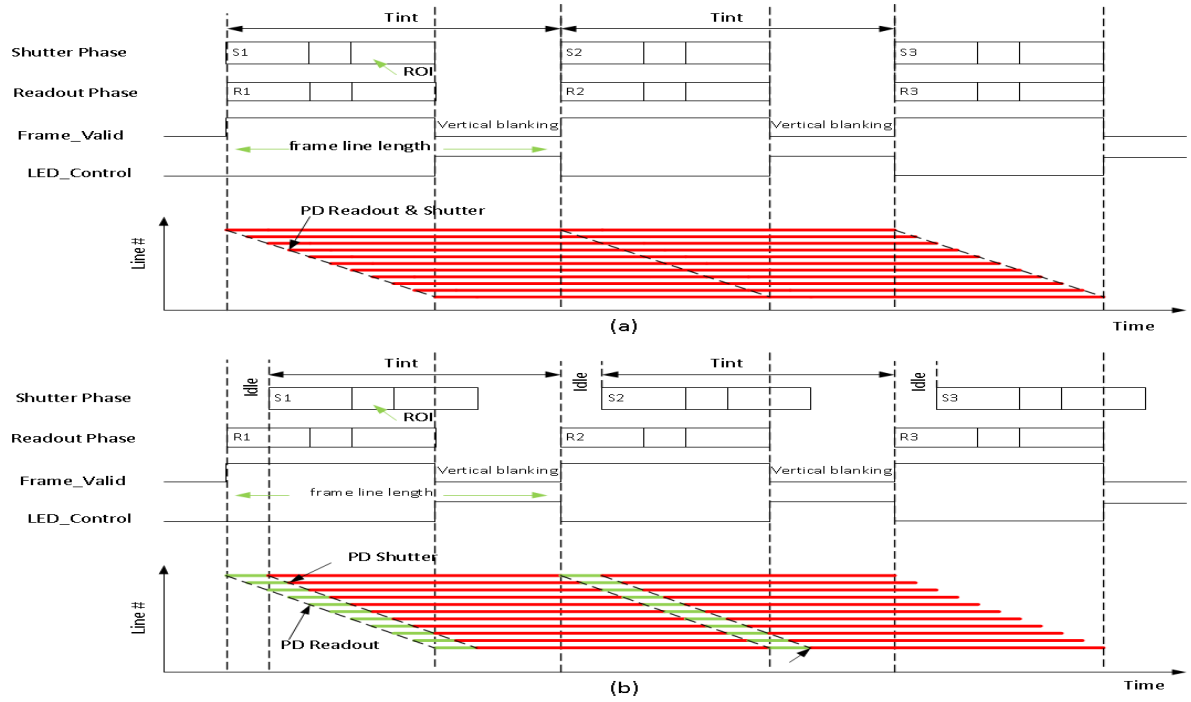


Figure 2. Pulsed LED Timing Control: (a) $T_{int} = T_{frame\_line\_length}$, (b) $T_{int} < T_{frame\_line\_length}$

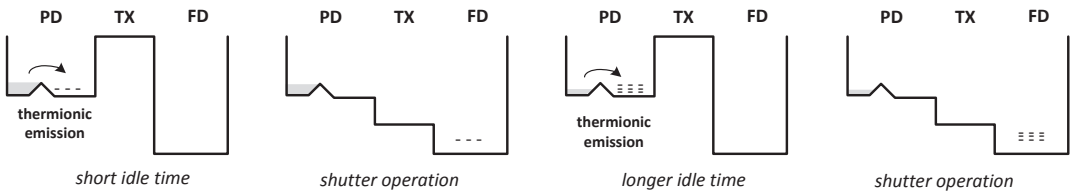


Figure 3. Thermionic Emission inside PD (a) short idle time, (b) longer idle time

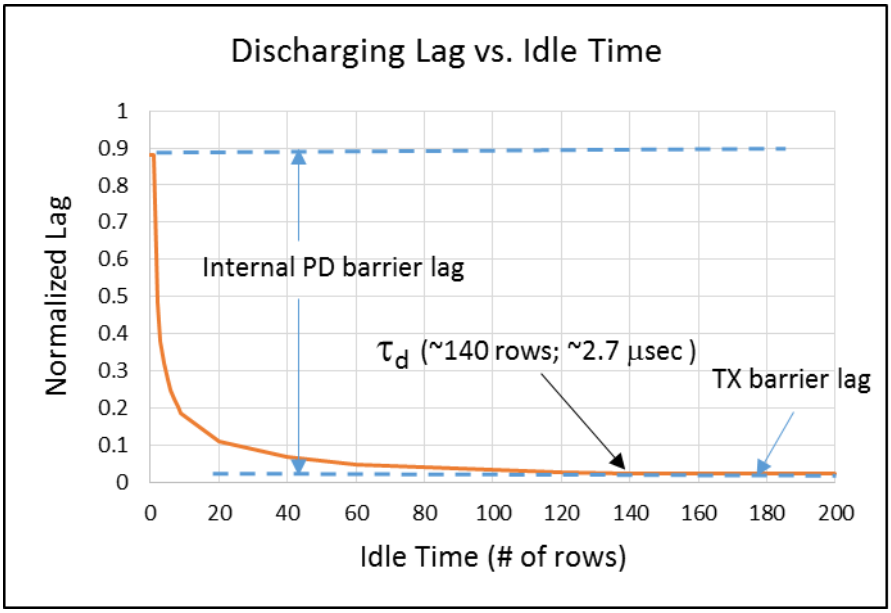
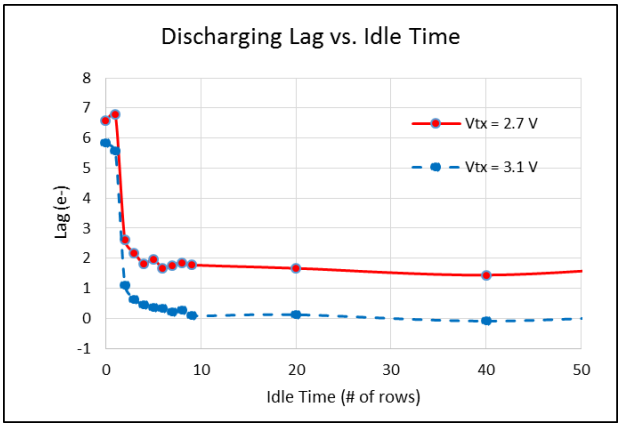
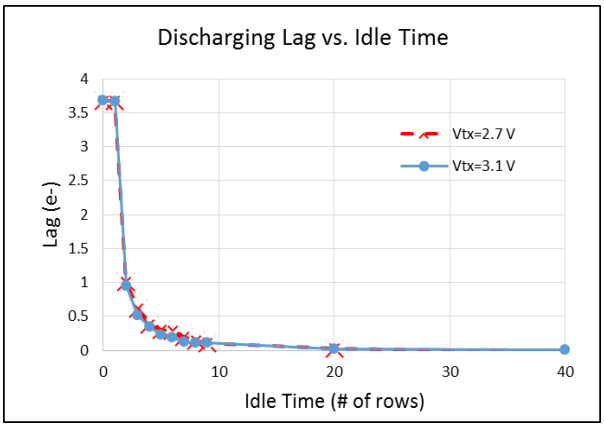


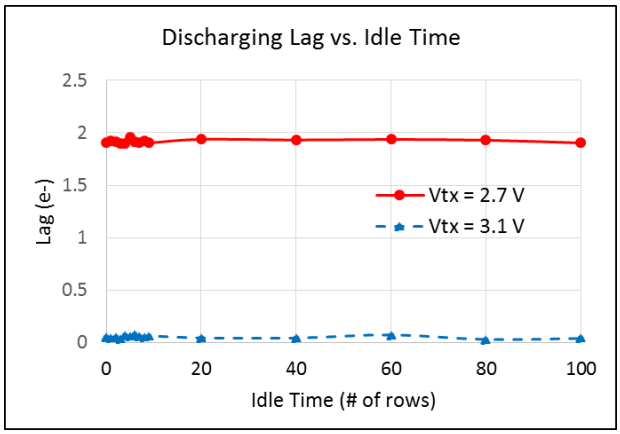
Figure 5. Lag vs. idle time plot and attendant features



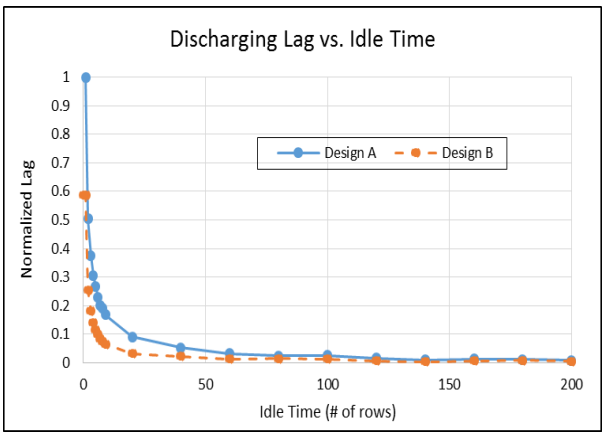
(a)



(b)



(c)



(d)

Figure 6. Lag vs. idle time data for various pixel designs: (a) PD barrier and TX barrier, (b) PD barrier only, (c) TX barrier only, (d) Different PD barriers