Back Side Illuminated High Dynamic Range 3.0 μ m Pixel Featuring Vertical p-n Junction Capacitance in A Deep Pinned Photodiode

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Introduction

High linear full well capacity (LFWC) is required to obtain high-fidelity high dynamic range performance in a single exposure high dynamic range (SEHDR[1)]) scheme in the CMOS image sensor. However, due to the deep pinned photo diode structure[2)] that is commonly used for back side illuminated devices, LFWC does not increase in proportion to the pixel size, since the pinning voltage increases as pixel size increases, while the supply voltage needs to be kept. In this paper, a high LFWC for 3.0 μ m pixel, which is relatively a large pixel in recent commercial BSI devices, using a latest 65nm BSI pixel process technology, is presented as a pixel for a 1/2.7", 2M-pixel CMOS image sensor[1)]. To increase the LFWC of the 3.0μm pixel, vertical p-n junction capacitance in the pinned photodiode is utilized. The developed pixel shows high performance, such as 77% peak QE, LFWC of 40ke$^-$, blooming and image lag free, and average dark current of less than 25e$^-$/s/pixel at 60°C.

PPD structure

A Pinned photo diode (PPD) structure of the pixel is shown in Fig. 1(b). In the presented structure, P-type layer is formed in the center of PPD, like a P-type pixel isolation layer, to have additional junction capacitance to boost LFWC. The split photo diode structure[3)] which has 2 sets of PPD and transfer gate and one floating diffusion node per pixel is shown in the Fig 1(c) for comparison. The stratified PPD structure[4)] which has vertically stacked P-type layers is considered as a reference of this type of PPD structure. Fig. 2 shows an example of electrostatic potential profiles with capacitance components along the lines of a - a' and b - b' in Fig.1 for the conventional type PPD and the presented one. Fig 2 also shows schematic views of p-n junction regions, the depletion layer widths (Wd) and their space charge density to visualize the difference between the two PPD structures. In the simple P$^+$N step junction model, Wd in PPD is expressed as Eq. (1) where ε is the semiconductor dielectric constant; Vpin the pinning voltage which makes PPD fully depleted; Nd the N dopant concertation; and φbi the built-in potential, respectively.

$$W_d = \sqrt{\frac{2\epsilon(\varphi_{bi}+V_{pin})}{qN_d}} \qquad (1)$$

As is shown in the right figure of Fig.2, the Wd (fully depleted region) becomes narrower in the presented structure (b) due to the P-type layer. Thus, Vpin to make PPD fully depleted can be lower compared to the conventional structure(a) with the same N dopant. This means that this structure allows to increase the N dopant (Nd) to boost LFWC with the same Vpin as that of the conventional PPD. Figure 3 shows an example of electrostatic potential in 2D device simulation for the proposed PPD structure to confirm potential modulation in BSI in different pixel sizes. It is confirmed that the location of potential peak shifts deeper and the peak potential increases as pixel size increases. This suggests that it is difficult to boost LFWC with a large PPD by increasing the N dopant, while Vpin and/or supply voltage is kept.

Characterization Results

Fig. 4 shows a schematic diagram of the pixel configuration to enable the SEHDR function, where three conversion gains can be selected[1]. A photo-electron conversion plot for this pixel is shown in Fig 5. LFWC of 40 ke$^-$ and FWC of 45ke$^-$ have been obtained with good linearity. In this paper, LFWC is defined with a photon shot noise peak and FWC is defined with the maximum output signal. Table 1 summarizes the pixel performance characteristics of a prototype sample for the 2M pixel sensor of Ref.1. As shown in Fig. 6 and 7, no degradation of key optical performances, such as quantum efficiency, angular response uniformity, are observed, despite the p-type layer formation in PPD. Fig. 6 shows an angular response of a green pixel in the Bayer configuration. Angular responses for both horizontal and vertical directions show no significant difference. Fig. 7 shows a QE plot for this pixel.

Conclusion

We have developed a back side illuminated 3.0 μm pixel featuring high LFWC which is realized by introducing a p-type layer in the deep PPD to create additional junction capacitance. 92dB dynamic range in the SE HDR mode without any key performance degradation has been obtained. The achieved LWFC significantly exceeds the trend of the saturation signal [5].

Reference

1) N. Yoshimura, et al., " *A 87dB Single Exposure Dynamic Range CMOS Image Sensor with a 3.0um Triple Conversion Gain Pixel* ", in Proc, 2017 International Image Sensor Workshop, Hiroshima, Japan May30-June2, 2017
2) N. Teranishi, " *Effect and Limitation of Pinned Photodiode* ", IEEE T-ED, Vol. 63, No. 1,pp.10-15, January 2016
3) M. Kobayashi, et al, " *A Low Noise and High Sensitivity Image Sensor with Imaging and Phase-Difference Detection AF in All Pixels*", in Proc, 2015 International Image Sensor Workshop, Vaals, The Netherlands 8-11 June, 2015
4) Y. Lim, " *Stratified Photodiode a New Concept for Small Size-High Performance CMOS Image Sensor Pixels* ", in Proc, 2007 International Image Sensor Workshop, Ogunquit Maine, USA June 7-10, 2007
5) Data source : www.sensorgen.inf

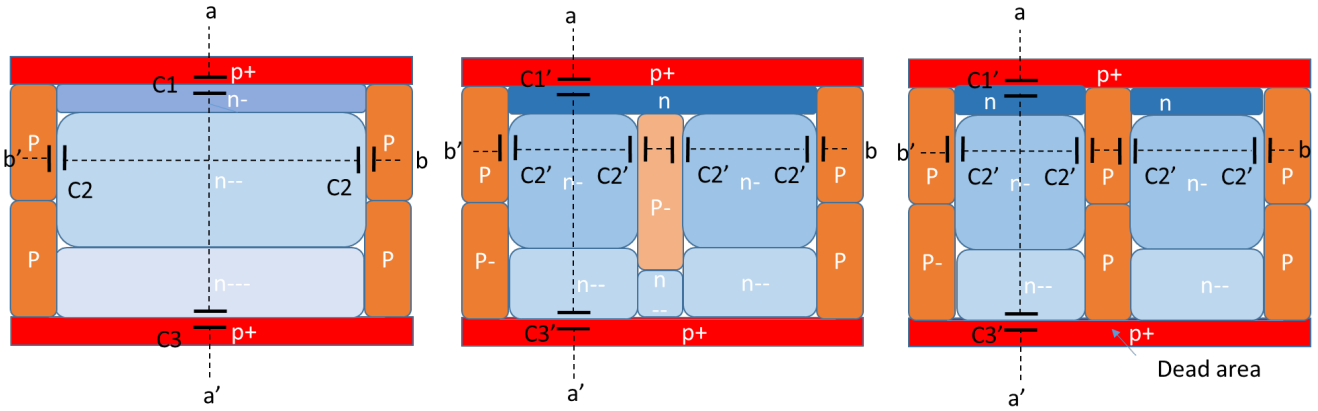


Fig. 1. Cross-sectional view of possible deep PPD structures for 3um BSI.
The parasitic junction capacitance of C1...C3' is illustrated along the cutlines a-a' and b-b'.

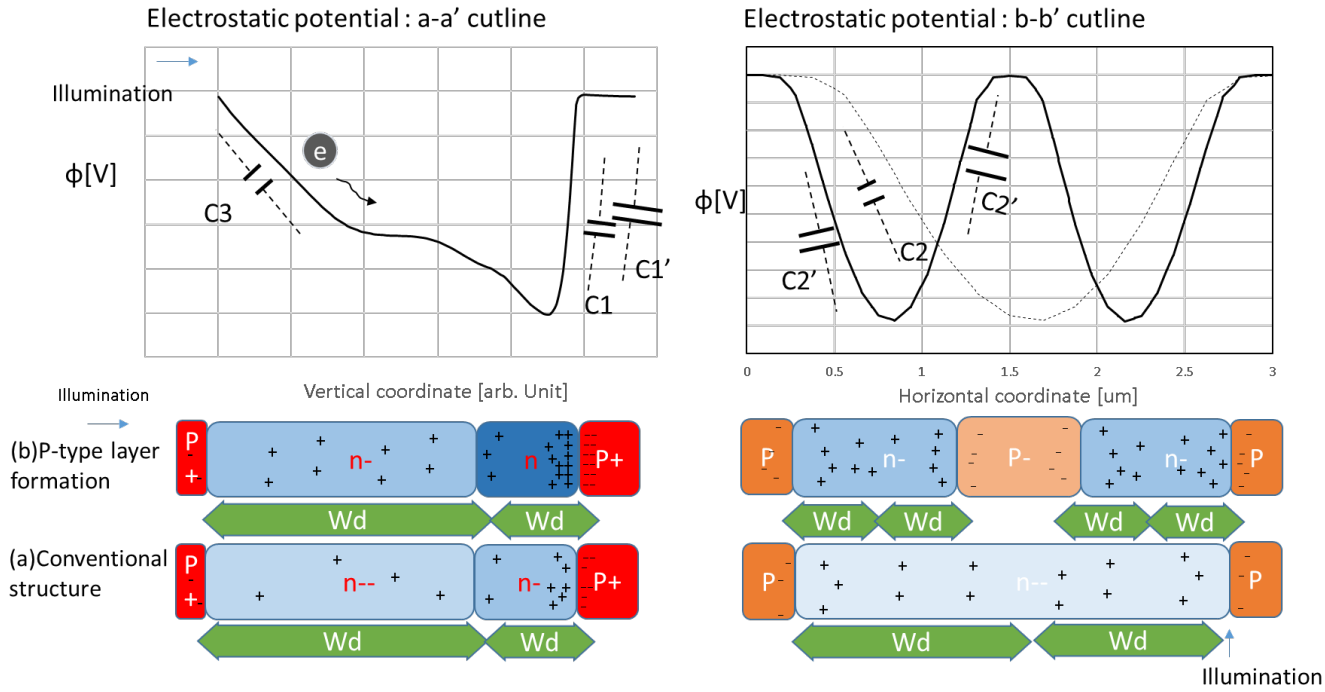
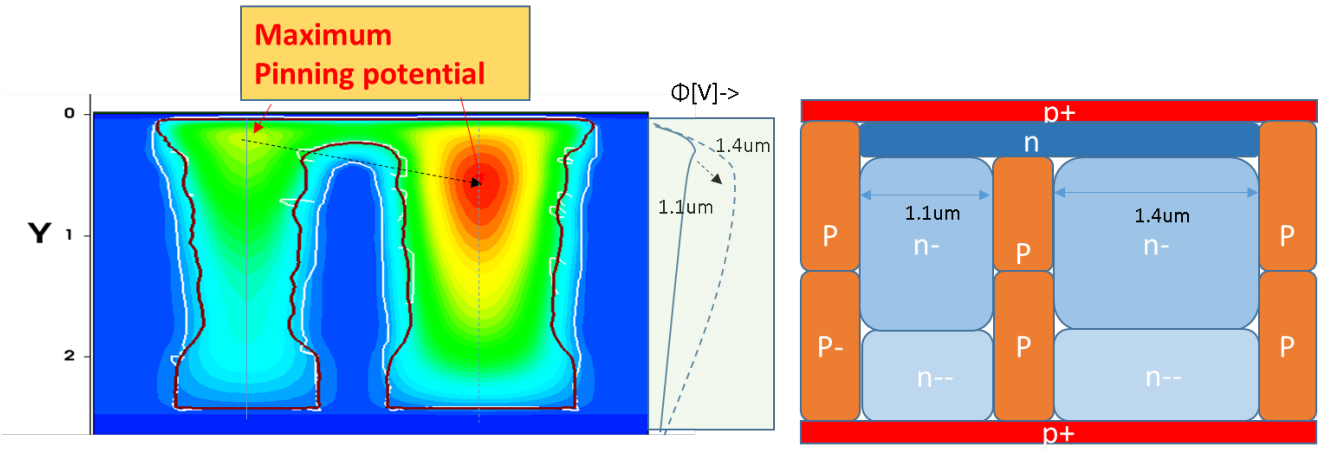


Fig. 2. An example of electrostatic potential profile, p-n junction region, space charge and depleted region (Wd)
(left : Vertical profile along the cutline a-a' of Fig.1 , assuming conventional structure has similar potential profile by doping adjustment.
right: Horizontal profile along the cutline b-b' of Fig.1, the doted line is for the conventional structure)



a) The electrostatic potential in 2D device simulation and its vertical profile at the center of PPD
(left : L=1.1um pixel, right: L=1.4um)

b) Doping profile model

Fig 3. An example of electrostatic potential in 2D device simulation using a P-layer formation model to confirm potential modulation in different pixel sizes.
Vpin is larger and the location of the maximum potential is deeper with a bigger pixel.

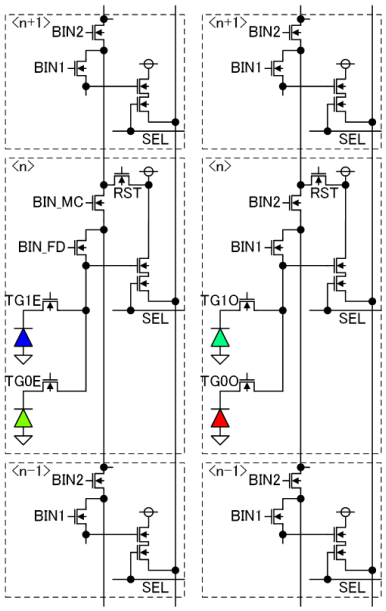


Fig. 4. Schematic view of SEHDR pixel circuit

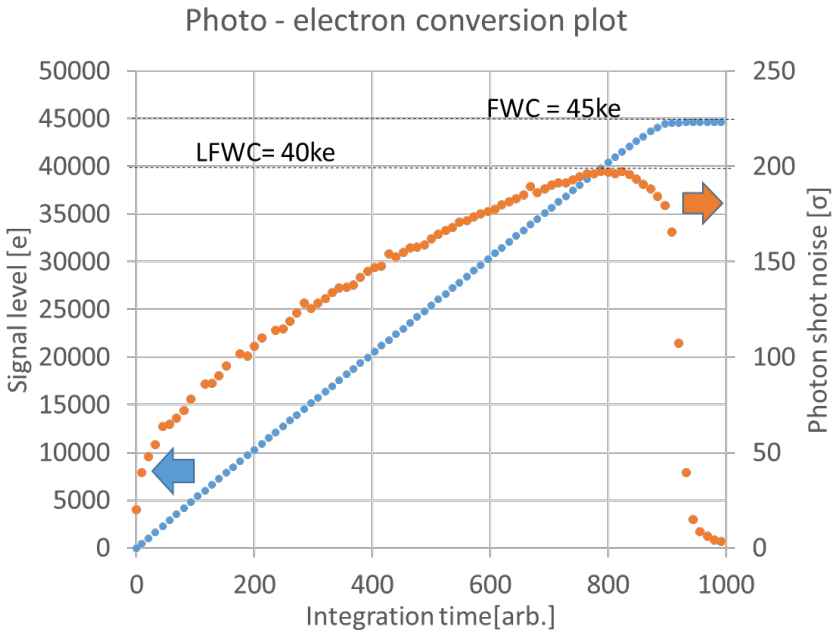


Fig. 5. Photo – electron conversion plot
(signal out [e] vs integration time)

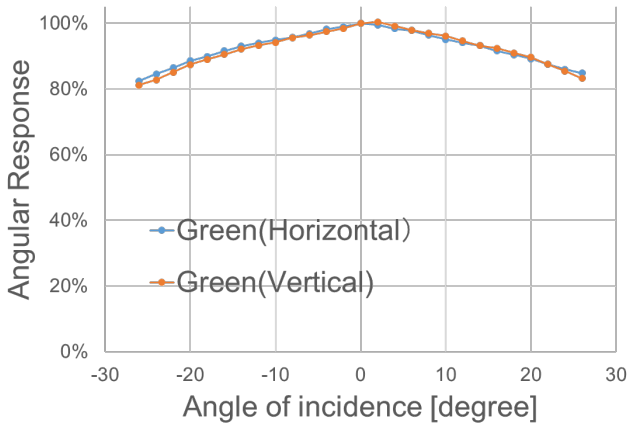


Fig. 6. G signal angular response in H/V directions @530nm

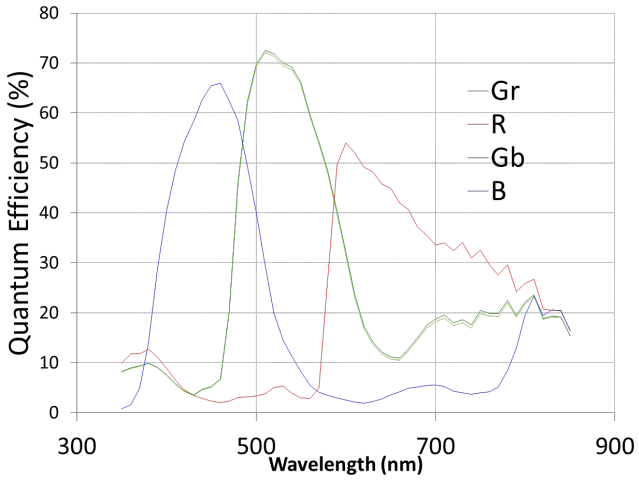


Fig. 7. QE plot (Glass lid transmittance included)

Table 1 . 3.0um back side illuminated pixel characteristic

Process 65nm BSI							
Pixel size	3.0um x 3.0um	FWC	45Ke$^-$	Noise floor	1.1 e$^-$	Angular response @±20° (H & V)	>90.4%
Linear full well	40ke$^-$	QE (G) max	78.8%	Dynamic range	91.3 dB	Dark current @60℃	25e$^-$/sec
Resposibity (5100k,CM500)	24ke$^-$ /lux.s	Image lag	<1e	SNR max	46 dB	Pixel operation voltage	2.8V