QLOG - logarithmic CMOS pixel with single electron detection capability

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ABSTRACT

In this paper, we present a new logarithmic pixel design currently under development at New Imaging Technologies SA (NIT). This new logarithmic pixel design uses charge domain signal logarithmic compression and charge transfer based signal readout. This structure gives a linear response at low light condition and logarithmic response at high light condition. The charge transfer readout suppresses efficiently the KTC noise by using a true CDS at low light condition. At high light condition, thanks to charge domain logarithmic compression, it has been demonstrated that 3000 electrons should be enough to cover 120dB dynamic range with a mobile phone camera-like SNR over the whole dynamic range. This low electron count permits the use of ultra-small floating diffusion capacitance (sub-fF) without charge overflow. The resulting large conversion gain permits a simple single photon detection capability without complex sensor/system design. A first prototype sensor with 320x240 pixels has been implemented to validate this principle. The first results validate the logarithmic charge compression theory and the low readout noise due to charge transfer based readout.

1. Introduction

Silicon based low light level image sensors are critical for many low power, low cost and highly integrated vision systems for many applications where high sensitivity and wide dynamic range are two key parameters besides resolution, frame rate and power consumption. Logarithmic response pixel is particularly useful for such applications since it can produce a very wide dynamic range directly at pixel level without any processing. The instantaneous accommodation suppresses all the auto-exposure latency, problematic in fast changing environments. Compared to other HDR techniques, a logarithmic sensor can give a considerable system simplification, both on design and validation, thanks to its contrast indexed sensing and predictable behaviors under uncontrollable environments.

Traditional logarithmic pixel designs suffer from large FPN, image lag and poor low light performance[1][2][3]. The solar-cell mode photodiode based logarithmic pixel design developed by Institute of Telecom in France from where NIT has spined off has reduced considerably the FPN and removed the image lag[4][5][6]. Commercial products have been successfully developed for different markets. The sensitivity of such pixel, even highly improved compared to traditional logarithmic pixel, is only equivalent to 3T CMOS APS, which is not enough for the applications such as video surveillance. To resolve this issue, we have investigated a new pixel design called QLog where the logarithmic compression is applied directly to the collected charge, similar to what happens inside solar cell mode photodiode. But the fundamental difference is that the photodiode here is fully depleted at the beginning of the exposure. This full depletion possibility of the buried photodiode, associated with charge transfer mechanism, permits the suppression of KTC at low light conditions. At high light condition, the logarithmic compression at charge collection stage reduces considerably the total electron number required to cover a wide dynamic range.

Actually it seems difficult to reduce the noise of in-pixel source follower due to 1/f and RTS noises, increasing the conversion gain seems a more straight forward solution. It's quite obvious that if we can reduce the capacitance of the floating diffusion, then we can reduce the readout noise level to sub-electron range. Some research teams are engaged in this way and reported readout noise close to or less than 0.25 electron [7][8][9][10]. As demonstrated by [10], single electron detection with reasonable probability can be reached at 0.28 electron readout noise. So QLog pixel can permit to reduce the floating diffusion capacitance to the low value as required by single electron detection

without suffering from extremely low dynamic range. This approach doesn't need multi-frame accumulation such as presented by [11] to recover the dynamic range.

In the following sections, we will present the basic logarithmic charge compression with a simple theoretical model. Then we present a validation test chip with 320x240 pixels. We will compare the measured results with the theoretical model. A set of parameters of the pixel design will be deducted for future single electron detection capable pixel design with some conclusions.

2. Logarithmic photo charge compression

As shown in Fig. 1, a potential well is formed near silicon surface by a buried PN junction in order to collect the photo generated carriers. The free carriers in silicon have certain thermal kinetic energy when the temperature is not absolute zero. All the trapped free carriers have a probability to escape from this potential barrier, which is determined by their kinetic energy and the barrier height. This probability can be written as:

$$\eta e^{-\frac{qV_B}{kT}} \tag{1}$$

where η, q, V_B, k, T represent structure factor, elementary charge, potential barrier, Boltzmann constant and absolute temperature.

In this case, at the entrance of this potential well, we have 3 carrier movements: 1) carriers attracted from outside, 2) carriers generated by photons directly inside the potential well and 3) carriers escaping to outside. We can merge the movements 1) and 2), so the residual carrier number will be governed by the following differential equation:

$$\begin{aligned} dN &= (-N\eta e^{-\frac{qV_B}{kT}} + G)dt \\ V_B &= V_{B0} - \frac{qN}{C_{PD}} \end{aligned} \tag{2}$$

Where C_{PD}, V_{B0}, N, G represent photodiode capacitance, initial barrier height, and residual carrier number and carrier generation rate.

It's not possible to have a closed form solution to this equation. A numeric resolution with $\eta = 1, V_{PIN} = 0$ gives the residual carrier numbers versus photon flux as shown in Fig. 2. The residual charge number with a fixed integration time follows two regimes: 1) linear regime at low photo flux and 2) logarithmic regime at high photo flux. A sharp transition connects these 2 regimes together.

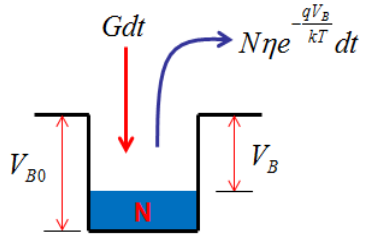

Figure 1. Carrier movements from and to a potential well.

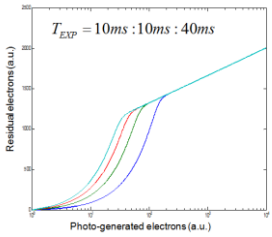

Figure 2. Residual carrier number inside the potential well in function of photon flux with different exposure times.

In a traditional pixel design, the barrier height of the collecting potential barrier is set as high as possible in order to minimize the non-linearity caused by carrier evaporation. In this case, the logarithmic regime is almost invisible since it exceeds the designed signal excursion. In our case, we minimize this barrier height in order to exploit the interesting logarithmic regime for charge compression. When a photodiode is used as carrier collecting device, then the barrier height can be set by the initial junction bias voltage plus its built-in potential. In a solar cell mode pixel design, a zero initial bias voltage pre-fills the photodiode's potential well with carriers, which gives a significant logarithmic response at the beginning. So the solar-cell based photodiode can be seen as a logarithmic charge compressing device in voltage mode where the effective potential barrier height is

measured as image signal. Here in QLog case, the potential well is depleted at the beginning of exposure, so a significant initial linear response is observed.

3. S/N modelling, DR and single electron detection

The noise modelling of this pixel design can be made separately for linear and logarithmic regimes. When the pixel is in the initial linear regime, the noise is simply composed of collected carrier shot noise and readout noise which will be ignored for simplicity. This noise can be written as:

$$n_e = \sqrt{N} \tag{3}$$

When the pixel is in logarithmic regime, the carrier movement will be symmetric and the noise becomes Johnson noise. In this case, the noise can be written as:

$$n_e = \frac{\sqrt{KTC_{PPD}}}{q} \tag{4}$$

As shown in Fig. 3, we can see that with a minimized barrier height and pinned photodiode capacitance, we can cover 120dB dynamic range with only 3425 electrons by using a conversion gain as high as 292uV/e. In order to get a readout noise of 0.28e, the SF noise should be less than 80uV. This is possible with a high performance CIS process and clever circuit designs. Fig. 4 gives the expected S/N ratio in linear and logarithmic regimes under this design condition.

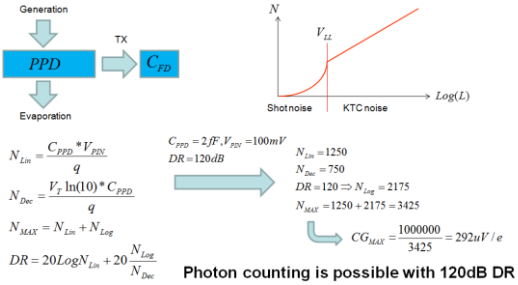

Figure 3. A set of design parameters to get single electron detection capability with 120dB dynamic range.

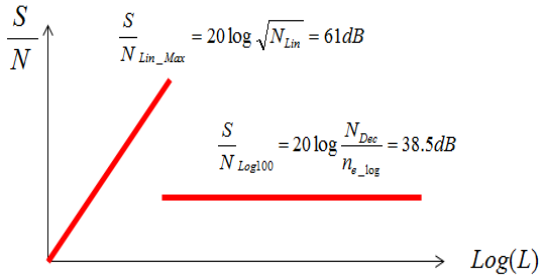

Figure 4. Expected S/N ratio for a QLOG pixel of Fig. 3.

4. Prototype test chip and measurement results

We have developed a buried photodiode and an efficient transfer gate in a standard 0.18um CMOS process. This test chip has been run many times during 3 years in order to define the correct recipe, including implant dose/energy and associated thermal process. A test chip with 320x240 pixels has been designed and fabricated. The photodiode area is of 9um^2 with near zero pinning voltage. Fig. 5 shows the measured response curves at 20ms exposure time. The linear to logarithmic transition matches the theoretical prediction. Fig. 6 shows the RMS and FPN noises in function of illumination level. The dark RMS noise is 6e with a 0dB readout gain. The operation dynamic range is over 120dB.

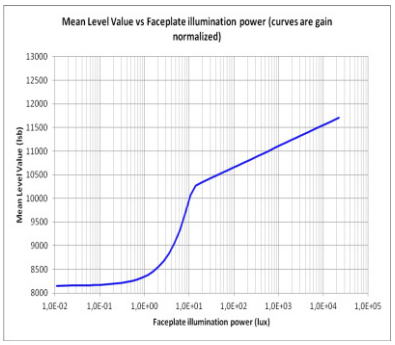

Figure 5. Measured response curves at 20ms exposure time.

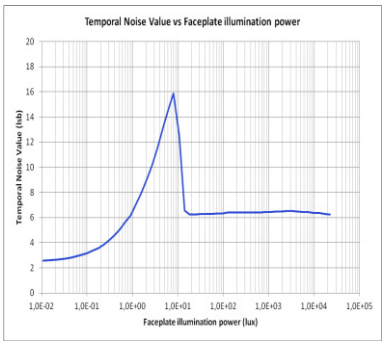

Figure 6. Measured RMS noise at 20ms exposure time.

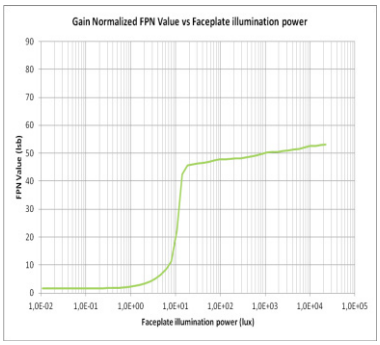

Figure 7. Measured FPN at 20ms exposure time.

There is a surged FPN when the photodiode goes into logarithmic regime as shown in Fig. 7. This FPN is almost constant and evaluated to about 150 electrons. The reasons and solutions to this FPN are still under investigation.

5. Conclusions

We have presented the new logarithmic pixel design QLog with wide dynamic range and low noise. This design can be seen as a charge domain extension from NIT's solar cell mode photodiode logarithmic pixel design. This new design benefices from fully depleted buried photodiode and charge transfer based readout in order to remove the KTC noise at low photon flux. The logarithmic compression at the photo generated carrier collection stage limits the number of carrier to cover a wide dynamic range. This highly reduced carrier number gives the possibility to use ultra small capacitance for the floating diffusion to get a high enough conversion gain to overcome the noise of the source follower transistor in order to obtain single carrier detection capability. Actually the residual FPN in logarithmic regime, the exposure-time and temperature dependent Lin-Log transition are currently under investigation.

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