Image Sensor With Multiple Sub-radix-2 SAR ADC Calibration and Residual Column Pattern Noise Correction

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This paper describes the optimization of column pattern noise in an APS-C optical format, 163Mpixel, 20fps CMOS image sensor designed in the TPSCo 65nm process. We determined that, for the combination of speed and resolution in this front-side illuminated process, a single-slope ADC approach was prohibitive due to counter speed and ramp distribution requirements. The architecture we choose was to segment the array into banks of columns, each with an associated serial ADC [1]. We used a SAR ADC for each bank of columns, which provided a good balance of power, size, and speed. To achieve the overall 3.33Gpixels/s readout rate, the sensor uses one ADC for every 104 pixel columns, with a total of 308 ADCs on the sensor. Image data is streamed out via a 32 lane LVDS output, each at 1.248Gbps. The sensor dynamic range is measured at 63.5dB, consuming 3.5W power consumption. Table 1 lists the sensor's specifications, and Figure 1 shows the sensor floor-plan.

Since mismatch between adjacent ADCs will appear as column-bank-wise pattern noise in low light conditions, linearity is absolutely essential in this architecture. The principal difficulty with SAR convertors is the requirement for capacitor matching and reference settling to ensure linearity and suppress mismatch. To address the linearity, we adopted a sub-radix-2 SAR architecture (Figure 2). The sub-radix-2 SAR architecture has inherent redundancy which relaxes these accuracy requirements compared to the standard radix-2 SAR case.[2] Background calibration determines the coefficients for each ADC to map the redundant bits to the final bit resolution. This process corrects the DNL and INL. These calibration coefficients are loaded into the sensor on power-up and the correction takes place individually for each ADC on chip. Figures 3 and 4 show the measured DNL results of an ADC in the array, pre- and post- calibration. The post-calibration DNL has no missing codes.

As expected, proper calibration of the ADCs was crucial to reducing the column-bank-wise pattern noise. Even with dark frame subtraction, the default bit weights left significant column offsets that were observable at low light levels. Applying the ADC calibration coefficients considerably reduced the residual column pattern. However, this still left a region at very low (<100 electrons) illumination where column pattern noise was visible. Since some application require high gain and extreme contrast enhancement, it was critical to eliminate this residual column pattern noise.

We found further reduction in column pattern noise by optimizing the matching of on chip reference generators. These reference generators were implemented per ADC readout channel as 7-bit switched capacitor DACs, and were intended to act as coarse equalization for the channel-to-channel offset of the ADCs. However, we found that tuning the analog offset with the DACs allowed us to also further reduce in the residual column pattern noise at low signal levels. The lower the initial analog channel to channel offsets were, prior to dark frame subtraction, the lower the resulting residual column pattern noise became after dark frame subtraction.

Figure 5 compares the results from a low-level (~100 DN) dark subtracted flat-field image with the following:

a) Un-calibrated ADC coefficents (i.e. ideal weights)
b) Calibrated ADC coefficients with no analog offset correction, and
c) Calibrated ADC coefficients with analog offset correction.

(Only a small section of the full image is shown here for clarity, covering 10 ADCs - Figure 5 also shows a plot of the column-wise average from images b) and c) for comparison). The analog offset correction further suppressed the peak-to-peak column-bank-wise pattern noise by approximately a factor of 2, pushing the remaining pattern noise significantly below the shot noise.

To investigate this effect further, we modeled a sample image using only ADC calibration to remove column pattern noise at low signal levels. This model simulated the calibration of 5 mismatched radix-1.85 ADCs for a flat-field image. After calibration and black level subtraction, each ADCs performance meets the definition of 12 bit performance. Even so, column pattern noise still appears at lower signal levels. The pattern noise is due to the remnant sub-12-bit INL differences between the ADCs, which are still visible when the noise is low. This situation is similar to the visibility of row-noise, where the rule of thumb is that row-correlated noise is visible at levels 10-20x smaller than the random noise level.

In addition to using a precision analog offset prior to the ADC to cancel the ADC offsets, there are several other methods to further reduce the pattern noise below the point of visibility. One approach is to spatially dither pixel columns across ADCs boundaries. This requires building a switching matrix between the pixel columns and the ADC inputs, which can be reconfigured on a row-by-row basis. If dark rows are available, the pattern noise can be further corrected by averaging the dark pixels in a column block and removing the residual differences between column blocks with digital subtraction. By adjusting the density of the offset application, sub-LSB offsets can be introduced that produce visibly pleasing alignment of the image offsets, without adding additional noise.

[1] D. Van Blerkom, et al., "Analysis of Front-end Multiplexing for Column Parallel Image Sensors," in *2011 International Image Sensor Workshop,* Hokkaido, Japan, June 2011.
[2] W. Liu et al., "A 12b 22.5/45MS/s 3.0mW 0.059mm2 CMOS SAR ADC Achieving over 90dB SFDR," ISSCC, 2010, pp. 380–381.

TABLE I
Device Specification Summary

Technology	TPSCo 65nm 1P 4M CMOS
Pixel size	1.5 um
Number pixles	163M
Active pixel array	15736 (H) x 10400 (V)
Active area	23.6mm x 15.6mm
Max frame rate	20FPS at full resolution
Input clock	26MHz
Output data	32 Lanes @ 1.248Gbps
Pixel rate	3.33Gpixel/s
ADC resolution	12 bit
Conversion gain	118uV/e-
Full well	6600e-
Readout Noise	4.43e- @ unity gain
Supply voltage	3.3V Analog / 1.2V Digital
Power Consumption	3.5W

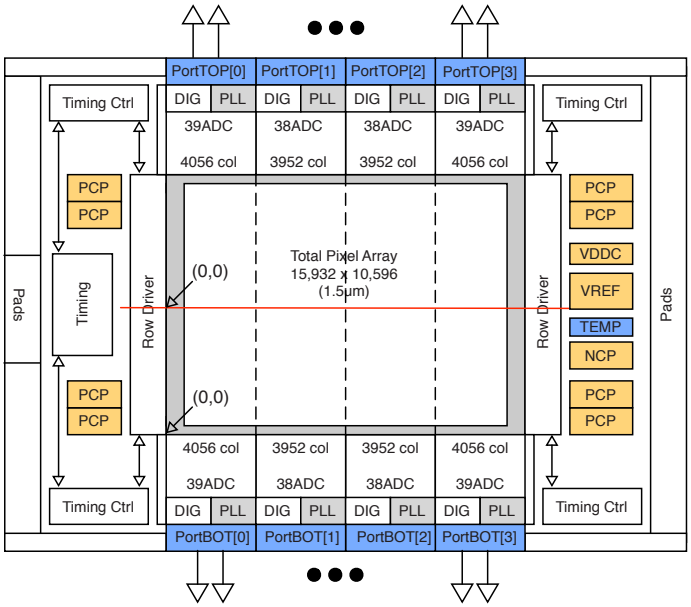


Figure 1 – 163 Mpix sensor floor-plan

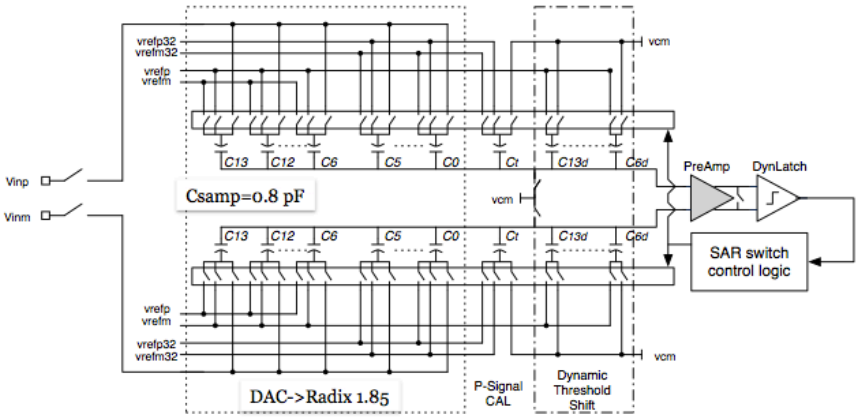


Figure 2 – Radix-1.85 ADC with Calibration

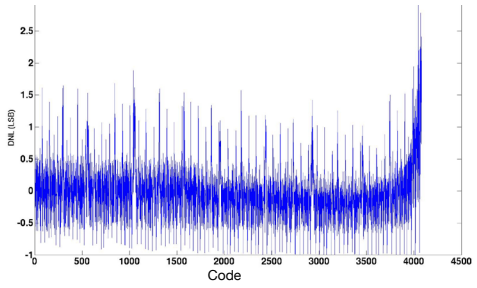


Figure 3 - pre-calibration DNL

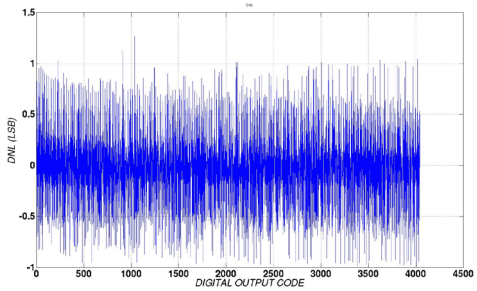
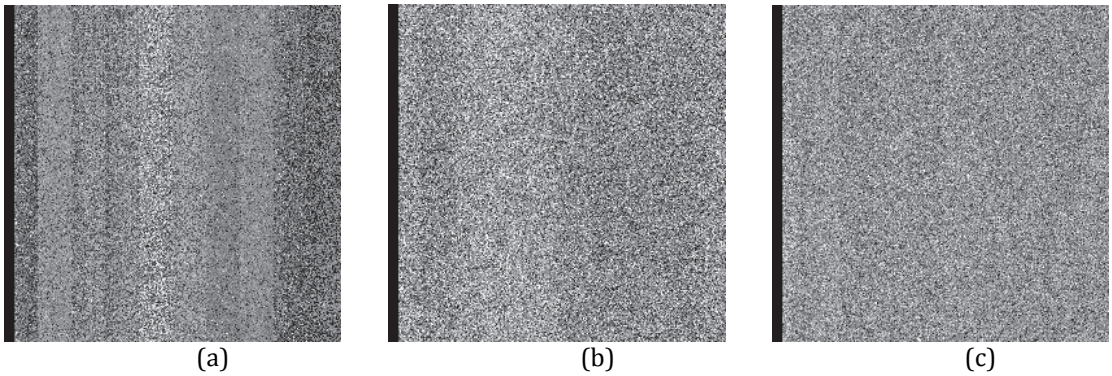
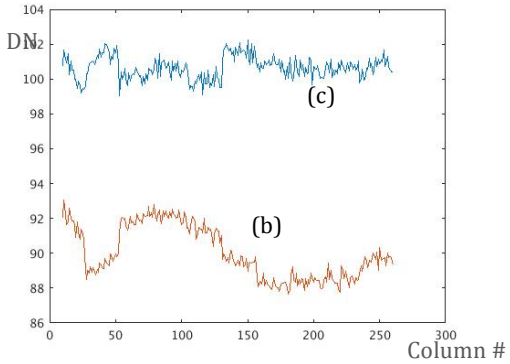


Figure 4 – post-calibration DNL

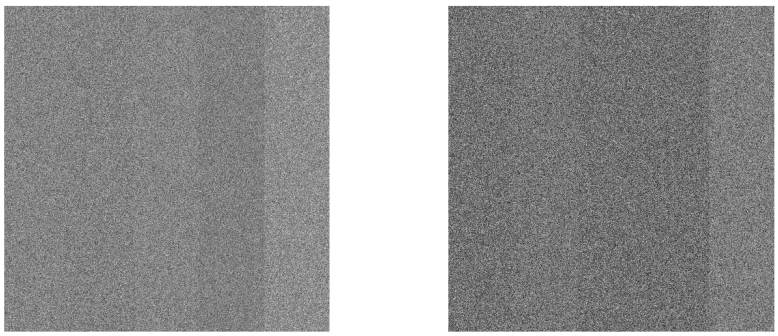


(a) (b) (c)



(d)

Figure 5 – Captured low-signal (60DN) flat-field image data
(color split, contrast enhanced & dark frame subtracted).
(a) No calibration (ideal weights); (b) Calibration but no analog offset correction; (c) Calibration with analog offset correction; and (d) column wise average plot of images (b) and (c)



(a) (b)

Figure 2 – Simulated contrast enhanced flat-field images at
(a) 10e- and (b) 20e- illumination