A 7-band CCD-in-CMOS multispectral TDI imager

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***Abstract*—We have developed a TDI sensor with 7 bands of 256 rows each using imec's CCD-in-CMOS technology. Each band uses individual on-chip sequencers and CCD drivers for the 5.4 µm four-phase TDI pixels. Line-by-line row selection per band, individual band selection and bi-directionality enable multispectral TDI. CCD bands operate continuously and time interleaved, and top or bottom outputs can be connected to shared column-parallel delta-sigma ADCs through a column line. ADC outputs are serialized to 32 1.2V LVDS outputs along with two clock signals. These outputs are capable of running at an aggregate of >50Gb/s using on-chip PLLs.**

The sensor has been packaged in a ceramic PGA package. As a proof-of-concept, an RGB butcher-brick filter has been applied to the glass lid of the sensor to enable multicolor TDI. The sensor has also been integrated into a custom CoaXPress camera.

The TDI sensor chip consumes 2.5W at full speed. Two pixel variations have been used. A high gain pixel achieves 10 electrons rms read noise and a full well of 12800 electrons rms with a conversion gain of 62 µV/e. A low gain pixel achieves 40 electrons rms read noise and a full well of 31600 electrons rms with a conversion gain of 28 µV/e.

I. Introduction

Time Delay Integration (TDI) imaging, commonly implemented in CCD technology, allows an increase of sensitivity by moving and integrating collected photo-charge in a CCD array synchronously to and along the track of a moving scene. Since readout only occurs at the end of the array, little read noise is added. CCD technology does not allow for ADC integration in the same die, and comes with speed and power bottlenecks. Moreover, the inability of CCD to read parts of the array – unlike CMOS imagers – makes the integration of multiband TDI difficult.

Integrated TDI sensors can also be realized without CCD technology for a low number of TDI stages (rows), taking advantage of improving CMOS pixel technology and ADCs [3, 4, 5]. Despite these improvements, digital TDI solutions with larger numbers of rows (e.g. >8) result in excessive readout noise and power consumption, since every TDI row needs to be read as opposed to only the output stage.

To address these issues we have developed a CCD-in-CMOS process integrating CCD pixels in a 130nm BSI CMOS process (Figure 1) [1]. Efficient charge transfer of CCD pixels is combined with CMOS high-speed and low-power electronics on the same wafer. Measurements done on a pixel test chip show a peak QE of 89%, correct CCD operation up to 800 kHz line rate, dark current of 3.5nA/cm^2 at room temperature and a CTI of $<5\cdot10^{-5}$ up to 800 kHz [2].

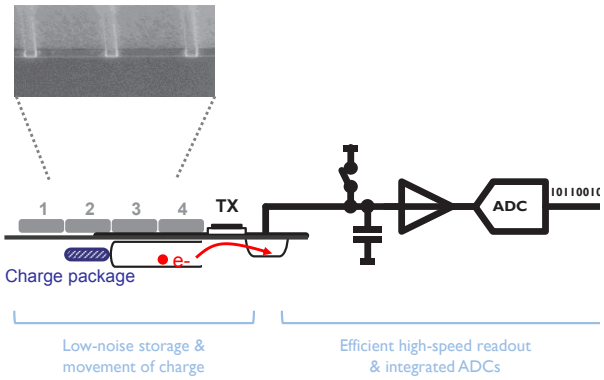

Fig. 1. CCD in CMOS concept

In this paper we describe a chip which combines these pixels with a versatile pixel controller, pixel drivers, high speed column ADCs and a high speed digital data transmitter. The chip is designed to integrate seven CCD pixel arrays (bands) with 256 rows and 4096 columns of 5.4 µm CCD pixels per band. This is done to develop a multi-spectral sensor, where each band is designed for a specific region in the UV to NIR spectrum

All bands are read by the same set of delta-sigma column ADCs. The outputs of the ADCs are serialized to 32 LVDS channels, each one capable of running at 1.6Gbps. Each band can be controlled independently in both directions, and the number of CCD rows used in each band is also programmable.

The paper is organized as follows. Section II will introduce the different building blocks. Section III explains the measurement set-up and the measurement results. Finally Section IV concludes the paper.

II. Chip Architecture

Figure 2 shows a block diagram of the chip. We briefly discuss the different building blocks: the chip controller together with the band sequencers, the pixel drivers, the ADCs and the data transmitters. The pixels are described in detail in [2].

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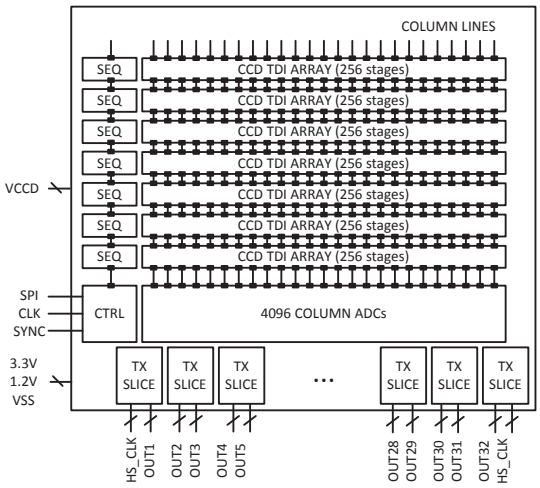


Fig. 2. Block diagram of the chip

A. Digital Control

The chip is controlled via an SPI interface, a clock signal and a signal (SYNC in Fig 2) used to enable the CCD operation. The SPI interface is linked to a set of digital registers on the chip. These registers control all the chip's building blocks.

The digital control consists of two sub-blocks: the *main controller* and the *band sequencers*. The *main controller* serves as the main SPI hub, controls the distribution of scan chain data and sequences the ADC and data transmitter operation.

The operation of the CCD arrays is controlled by the *band sequencers*. Each band has its own sequencer which can be programmed independently. All sequencers are identical copies of the same basic circuit. The *band sequencers* control the operation of the CCD pixels, the output stages in each band and the synchronization with the column ADCs. The CCD charge can be directed in both directions (upper or lower side of the arrays in Fig. 2) and read from either of the two output stages (upper or lower). The number of rows used for CCD operation can also be defined via the band sequencer from 1 to 256. The CCD rows which are not read are clocked towards the output stage which is not being read. That output stage is continuously connected to the positive supply to avoid blooming. Because there is only one set of column ADCs for the seven bands, the sequencers must be carefully programmed to avoid conflicts, i.e. multiple bands trying to operate the ADCs at the same time.

B. Pixel Drivers

The outputs of the band sequencers have to drive the CCD pixels. This requires a larger voltage swing than allowed by the standard digital cells in this technology. It also requires driving a large load (4096 columns of pixels) and control of the rise and fall times. Fig. 3 shows a simplified schematic of these pixel drivers. They consist of CMOS inverters with falling edge slope control. The sizes of the transistors are optimized for driving the pixel loads at a maximum line rate of 300 kHz.

C. Analog-to-Digital Converters

The column ADCs are inverter-based incremental delta-sigma ADCs. They are designed for an input full range of 1V. The range can be adjusted to match the output range of the output stages of the CCD bands. Correlated Double Sampling (CDS) operation is performed in the digital domain.

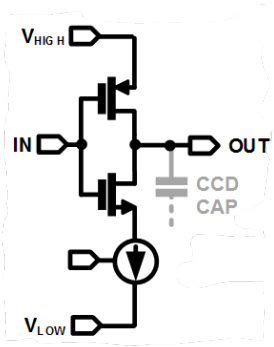


Fig. 3. Schematic drawing of the pixel drivers

The resolution of the ADC can be controlled by the number of conversion steps used (equivalent to the oversampling ratio in a conventional delta-sigma ADC). The ADCs in this chip were designed for a maximum SNR of 12 bits and a maximum speed of 1MS/s.

D. Digital data transmitter

Each set of 128 columns is assigned to one output data channel. Each channel consists of a *digital readout block*, a *serializer* and a *differential LVDS transmitter*. Two channels make one transmitter slice, shown as TX slice in Fig 2. Each transmitter slice contains one PLL, which means that two channels share the same PLL. All channels and PLLs are independently programmable.

The *digital readout block* has several functions. The first one is to interface between the ADC outputs and the serializer. The digital readout block can add (or remove) a fixed offset to the ADC outputs. A second function of the digital readout block is to generate test patterns which can be used to test the integrity of the data link. The most important function of this block is to control the operation of the serializer, be it with ADC or test pattern data. As long as the digital readout block does not receive the command to send data to the serializer, it puts "idle" words to the serializer inputs. The *main controller* indicates to the digital readout block when there is meaningful data to be transmitted (test or image data). At this point the readout block puts one "sync" word into the serializer input, followed by the data words.

The *serializer* consists of a shift register. The contents of all the bits in the register are loaded in parallel. The register is then operated at the output clock speed to shift all the bits one by one via the LVDS transmitter

The *differential LVDS transmitter* is designed to operate at 1.2V supply voltage. The common mode and peak to peak voltages on the differential 100 Ohm load are programmable.

III. Chip Measurements

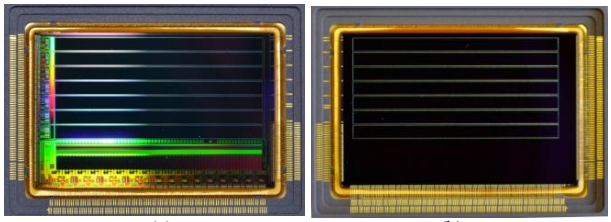
Two variants of the chip have been fabricated and evaluated. A front-side-illuminated (FSI) and a back-side-illuminated (BSI) version. They are shown in their packages in Fig. 4.

A custom micro-PGA ceramic package has developed for each version of the chip. The two packages share the same pin configuration so they can be used in the same evaluation set-ups and cameras.

A. Measurement set-up

The chips have been evaluated in a system consisting of a custom PCB where the chip is placed, a custom board to control

and measure all the chip supplies independently, a commercial FPGA development board and custom software for controlling the chip, performing measurements and analyzing data.



(a) (b)

Fig. 4. Packaged TDI sensors: (a) FSI version, (b) BSI version. The different building blocks are clearly visible in the FSI version (CCD bands, ADCs, pixel drivers, output data channels. The bands are also visible in the BSI version: the readout nodes of the bands are shielded by metal.

B. Measurement results

The performance of the digital data transmitter has been tested using one of the test patterns generated in the digital readout block. All channels are programmed and the output data is compared with the expected data in the FPGA or a PC. The target data rate of 1.6Gbps per channel was verified in this mode.

The ADCs are characterized via a dedicated test input. A voltage is applied at this input, which is buffered to all the ADCs at the same time. The measured SNR performance is 10 bits in average for all ADCs in one sample. The main reasons found for this discrepancy are due to parasitic effects in the quantizer of the ADC.

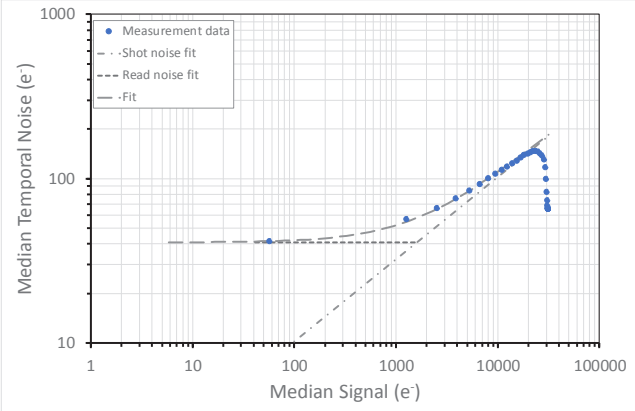
The operation of the digital band sequencers and the ADC digital control is verified via test output pins. The control signals from each *band sequencer*, as well as the signals from the *main controller* controlling the ADC and data transmitter can be independently sent to these test output pins. All the basic functionality was successfully tested in this way.

The operation of the pixel drivers can be verified by monitoring their outputs at the other side of the array via dedicated test output pins. An issue in the package prevents us from testing the drivers with the correct CCD operational voltages, but the basic functionality and rise and fall times have been verified to be as expected.

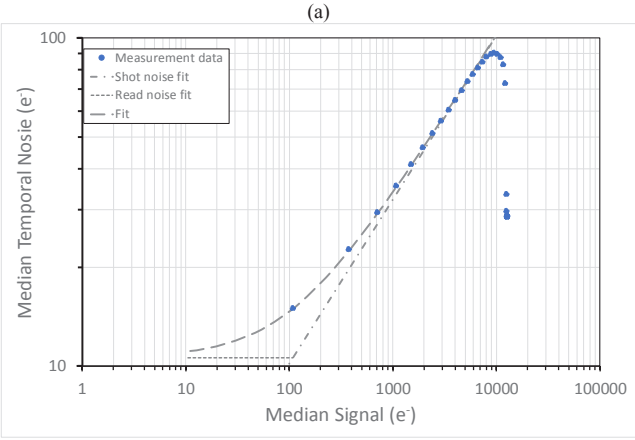
The performance of the pixels in the seven bands has been checked using the dark signal transfer curve, and by taking live images. We have not observed large differences in the performance of the bands within the same sensor and across sensors in the same batch.

Figure 5 shows the dark signal transfer curves for two pixel variations from the same lot. The ADC input range is optimized so that the full well is limited by the pixels and not the ADC. The measurements confirm the higher read noise than expected due to the higher than expected noise in the ADC. The pixel's charge to voltage factor (CVF) and full well capacity (FWC) are measured to match the designed values and is in line with the measurements in the pixel test vehicles reported in [2]. The values are reported in Table I.

A problem was found with the serial link when the ADCs and pixel are also enabled. The jitter in the channels increases to a level where the data cannot be read without errors. The chip needs to be operated at a lower speed by disabling the PLLs in the serializers in order to get correct data. That limits the maximum speed of the chip to a line rate of 43 kHz, about 7 times slower than the design target of 300 kHz. Nevertheless, the maximum speed of the CCD pixels can still be achieved by operating the pixels at full speed and skipping rows in the ADC and data transmission circuits. This is easily achievable thanks to the flexibility in the programming of the band sequencers.



(a)



(b)

Fig. 5. Dark Signal Transfer Curves for the (a) high full well and (b) high conversion gain pixel types.

The power consumption of the chip was measured to be 2.5W when all bands are enabled and working at the maximum line rate with the on-chip PLLs enabled. When the chip is operated with the PLLs disabled so that the image data can be correctly read by the FPGA the power consumption is 2.4W. Most of the power is consumed in the ADCs, followed by the LVDS drivers and the digital circuits (band sequencers and digital readout).

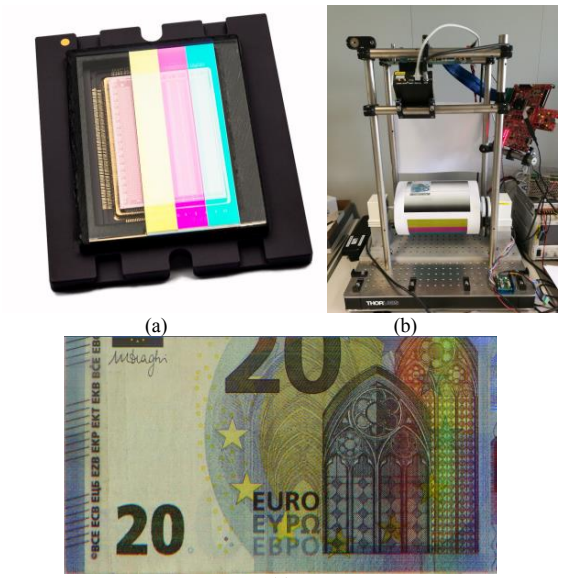
C. TDI operation with color filters

As a proof-of-concept, an RGB butcher-brick filter has been used as glass lid for the sensor, to enable multicolor TDI, although filters may be processed directly on the wafer as well [6]. Figure 6a shows a packaged chip with the color filters in the glass lids.

In order to test the TDI operation, a demo set-up has been built which consists of a rotating drum where the target is located, and either the development board or the camera is fixed above the drum to capture the image, as shown in Figure 6b. The rotating speed of the drum and the line rate of the sensor are then synchronized. Figure 6c shows an example of a picture taken in the rotating drum setup with a BSI sensor with the RGB color filters. The color image is reconstructed in software from the images obtained from the three bands.

TABLE I
SENSOR CHARACTERISTICS

Specification	This work	Ref [3]	Ref [4]	Ref [5]
Array size	4096 columns 256 rows	64 columns 40 rows	128 columns 64 rows	1024 columns 128 rows
Number of bands	7	1	1	1
Stage selection	1-by-1	N/A	N/A	Yes (CIS readout)
Bidirectional	Yes	N/A	N/A	Yes (CIS readout)
Pixel size	5.4 µm	13 µm	7.5 µm	15 µm
CVF (µV/e)	62 28	11	Between 10 and 15	N/A
FWC (e)	12800 31600	N/A	92000	N/A
Read Noise (e)	10 40	N/A	Between 20 and 30	N/A
Max line rate	43 kHz	N/A	15 kHz	3.9 kHz
ADC-on-chip	Yes	No	No	Yes
Power consumption	2.5W	N/A	N/A	290 mW
Technology	130nm BSI CCD-in-CMOS	180nm CCD-in-CMOS	150nm CCD-in-CMOS	180 nm CMOS
Communication interface	SPI	N/A	N/A	N/A
Output format	32x sLVDS	Analog	N/A	N/A
Supply voltages	-1.5V, 1.2V and 3.3V	> 3.6V for CCD	N/A	N/A



(c)

Fig. 6. (a) Sensor with RGB filters in the glass lid, (b) Rotating drum set-up, (c) color image obtained with the RGB sensor in the rotating drum set-up

D. TDI operation with a camera

The sensor has been integrated into a custom CoaXPress camera. Figure 7a shows the sensor in the camera, looking through the lens hole.

The camera has been integrated into the rotating drum setup and figure 7b shows a single band image captured with this setup.

Fig. 8. (a) The TDI sensor inside the camera, (b) single band image taken with the camera in the rotating drum set-up.

IV. CONCLUSION

We have designed and fabricated a single-chip multi-band TDI sensor using CCD-in-CMOS technology [1]. The chip integrates seven bands of 256 by 4096 CCD pixels, programmable controllers for each band, 4096 column ADCs and 32 digital data transmitters capable of operating at 1.6 Gbps each. We have demonstrated the operation of all the building blocks and we have obtained similar results in the pixel arrays as measured in the pixel test vehicle of [2].

The chip has two limitations with respect to the original design parameters: the ADC noise is higher than expected and the digital data transmitters cannot operate at full speed when the ADCs are also enabled. For both issues we have found solutions which require redesign of these blocks.

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