Charge-Coupled CMOS TDI Imager

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***Abstract*—A charge-coupled CMOS time delay and integration (TDI) imager is presented. CCD pixel arrays of varying sizes and configurations were monolithically integrated with CMOS peripheral circuits using a conventional 0.18 μm CMOS technology with custom CCD process modules. A 5 μm pixel variant with 256 TDI stages demonstrated a charge transfer efficiency (CTE) > 0.99999 per transfer and a full well capacity (FWC) > 30,000 electrons at a maximum TDI scan rate of 270 kHz. It also exhibited a non-linearity < 2%, a dark current density at 25°C of 3.7 nA/cm^2 and a peak responsivity of 14,000 (DN$_{12b}$)/(nJ/cm^2) at 670 nm with capabilities of stage selection, bi-directional scanning and anti-blooming (AB) protection. The developed imager shows strong potentials to replace the traditional CCD-TDI imager in demanding applications including machine vision and remote sensing.**

I. Introduction

Next to high volume consumer applications, CMOS image sensors have been rapidly displacing CCD image sensors in various niche markets. There is however another important type of imaging technique, TDI imaging, which is still predominantly implemented by the traditional CCD technology. The TDI imaging has been commonly used in demanding applications in which high-speed and high-sensitivity imaging capabilities are essential.

A CMOS approach to the CCD-type TDI has been disfavored mainly due to incomplete charge transfer associated with a gap between two adjacent poly-Si gate electrodes. As CMOS technology has continued to scale down, the minimum gap achievable has decreased in favor of charge transfer. Recently, several groups reported CCD-TDI implementation using a standard CMOS technology at multiple technology nodes [1-4].

In this work, we report on the architectural design of a test vehicle for the development of a charge-coupled TDI imager with CCD imaging core monolithically integrated with CMOS peripheral circuitry. We also discuss the technological development of custom CCD process modules successfully integrated into a conventional 0.18 μm CMOS technology, followed by measurement results of the test chip obtained to date in comparison with our traditional CCD-TDI camera performance.

II. Sensor Architecture

Figure 1 shows the optical micrograph of the fabricated die. The CCD imaging arrays contain 5 and 10 μm pixels, each of which consists of 256 and 64 TDI stages. Various pixel splits intended to optimize imager performance parameters including CTE, FWC, dark current density and linearity were included. Figure 2 illustrates one of the pixel configurations with alternating column-wise channel stop (shallow trench isolation, STI) and gated AB structures in odd and even pixels. Here, a lateral AB (LAB) structure was employed for future backside illumination (BSI). The test vehicle also includes pixel variants designed for the study of post-radiation exposure effects for space applications. In addition, the sensor design supports one dimensional stitching to construct a higher resolution format than the 4k pixels of the test chip.

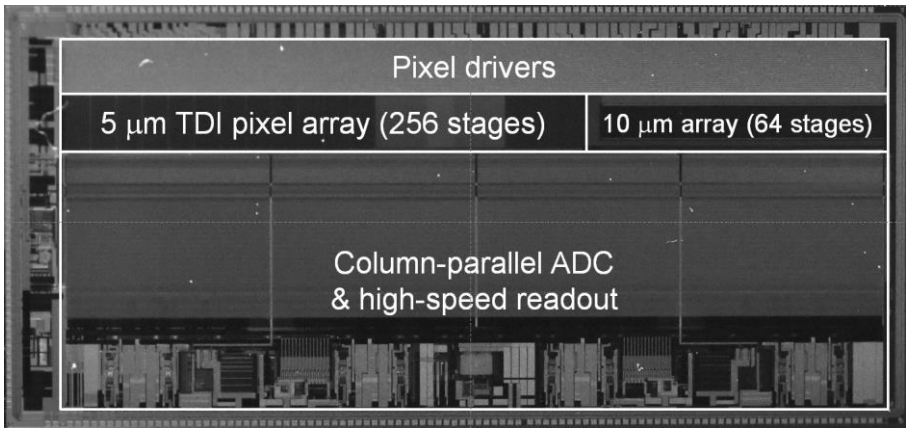

Figure 1. Optical micrograph of the fabricated test vehicle.

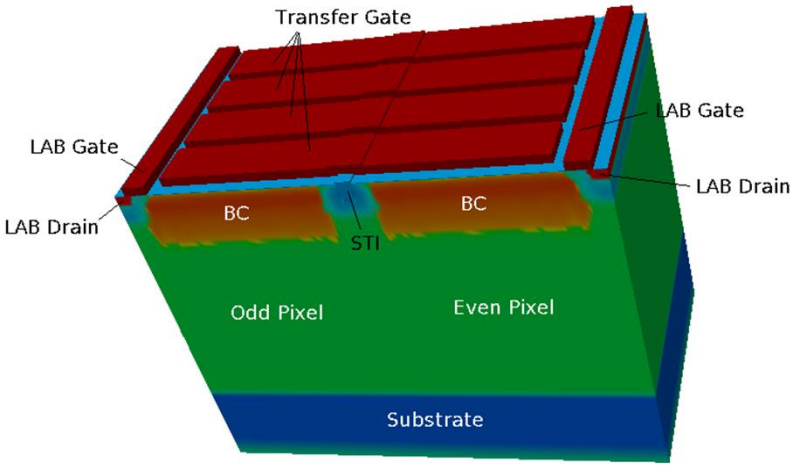

Figure 2. LAB pixel architecture.

At the top and bottom of the arrays, there are output stages (sense node, reset and source follower) for bi-directional scanning operation. Both the output stages are multiplexed to column-parallel ADCs located below the arrays. Above the arrays, pixel clock drivers are located, from which the poly gates are vertically strapped with metal buses for high-speed operation. The pixel drivers were built using a triple well process to provide a negative voltage for a clock low level for pinning operation for dark current reduction. The drivers were also designed to have controls for clock edge speeds to fine-tune the CTE. An on-chip timing core supports a stage-selection capability, i.e., 64/128/192/256 and 16/32/48/64 TDI stages selectable for the 5 and 10 μm arrays, respectively. It also provides options for different clocking schemes, e.g., continuous clocking typically required in earth observation applications.

III. Technology Development

The CCD-TDI image sensor has a large active area basically free of structures but high-density pixel electrodes with small gaps. This is atypical for a standard CMOS technology and can cause several issues including (1) nitride erosion and/or oxide dishing during a chemical-mechanical polishing (CMP) step for active-area definition, (2) failures due to high gate leakage and/or gate leakage-induced issues particularly when the gates are negatively clocked for pinning, and (3) poly shorts due to narrow gaps between the charge transfer electrodes. Prior to test chip fabrication, we therefore started CCD technology development by performing short-loop experiments using generic test structures (comb, serpentine and cross-bridge structures) for failure mode detection and design rule validation. Based on lessons learned, not only process modifications but also design considerations were successfully implemented for the test chip. We also used a dual oxide process, i.e., a thick oxide in the pixel region to address the gate leakage issues whereas a thin oxide in the circuit region to reduce power consumption. The thick oxide in the pixel region also provides voltage margins to increase a CCD clock swing which can help to improve the CTE.

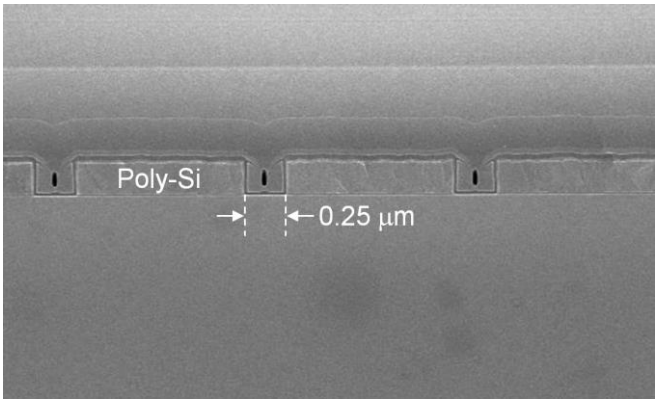

Figure 3. SEM cross-section of the fabricated CCD pixel in the along-track direction.

Buried channel (BC) operation is indispensable for complete charge transfer. However, BC implant is not readily available in a standard CMOS technology, which must be developed and integrated without extra thermal cycle(s) such that it does not affect existing CMOS processes. In addition, advanced lithographical techniques were employed in previous research to achieve smaller poly gaps [1-3]; the larger the gap is, the deeper the potential pocket is created in the gap, which degrades the CTE. However, those techniques are not readily accessible in silicon foundries. We, instead, used a deep BC to reduce a depth of the potential pocket [4] formed in a 0.25 μm gap which is standard at the 0.18 μm technology node. The SEM cross-sectional view of the fabricated CCD pixel in the along-track direction (i.e., along charge transfer direction) is presented in Figure 3. Various BC implant conditions were also investigated to achieve both good CTE and FWC. Secondary ion mass spectrometry (SIMS) profiles were taken for one of the BC implant conditions and the calibration of Monte Carlo implantation simulation was performed for pixel design as shown in Figure 4.

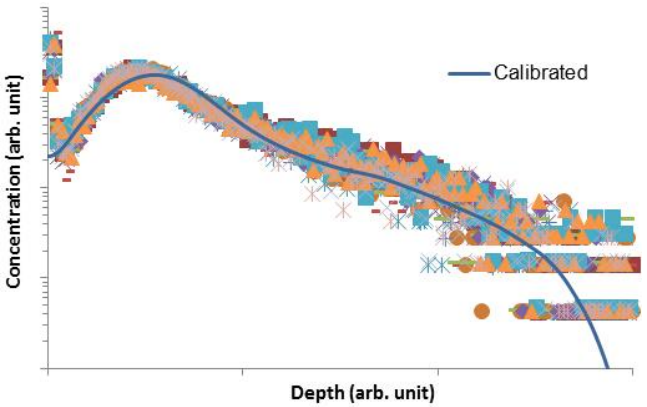

Figure 4. Calibration of Monte Carlo implantation simulation to BC SIMS profiles.

IV. Test Results

Among various design splits, the test results of a 5 µm LAB pixel (its architecture shown in Figure 2) with 256 TDI stages are presented here. When a deep BC is used as in our approach, achieving both good CTE and FWC simultaneously is challenging because it reduces not only the potential pocket in the poly gap but also the FWC. The test pixel fabricated using one of the BC implant splits successfully demonstrated a FWC > 30,000 electrons while achieving a CTE > 0.99999 per transfer at a TDI scan rate of 270 kHz for various signal levels, which was characterized using the extended pixel edge response (EPER) method [5] as shown in Figure 5. Here, charge is transferred from right to left. The amount of deferred charge in the first overclocked row is also shown in the inset.

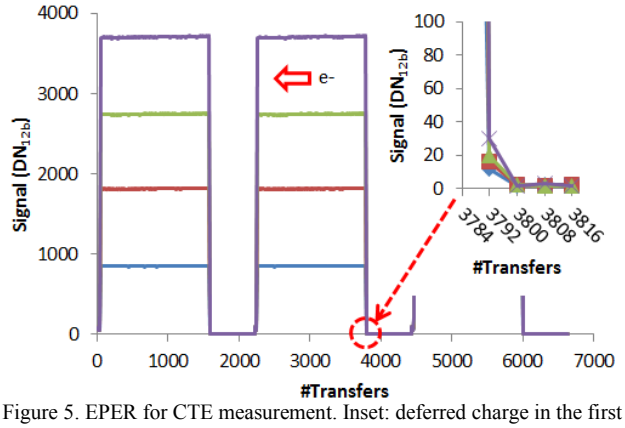

Figure 5. EPER for CTE measurement. Inset: deferred charge in the first overclocked row.

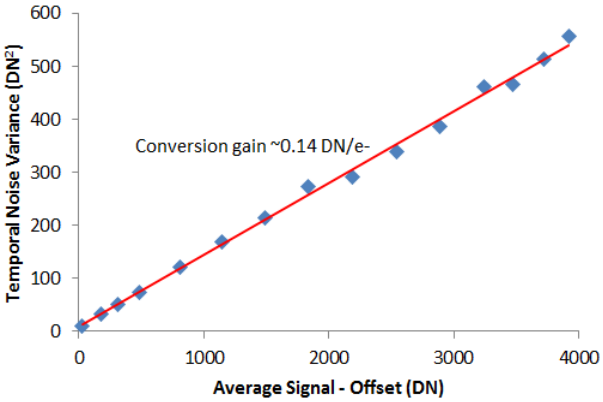

Figure 6. PTC.

The pixel output exhibited a non-linearity < 2%. The conversion gain of ~0.14 DN/e- was extracted using the photon transfer curve (PTC) presented in Figure 6. The temperature dependence of the dark current is provided in Figure 7. The dark current density at 25°C is 3.7 nA/cm^2. The activation energy (E_a) of ~0.6 eV extracted from the Arrhenius relationship is close to half the silicon band gap, which is indicative of the conventional Shockley-Read-Hall (SRH) mechanism as a source of the dark current. The spectral responsivity and quantum efficiency (QE) is presented in Figure 8. It shows a peak responsivity of 14,000 (DN$_{12b}$)/(nJ/cm^2) at 670 nm. The test vehicle also demonstrated capabilities of stage selection, bi-directional scanning and AB protection. A TDI drum image captured at a scan rate of 79 kHz is provided in Figure 9.

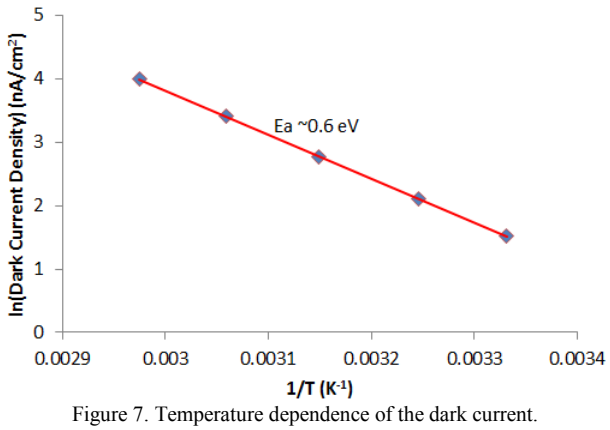

Figure 7. Temperature dependence of the dark current.

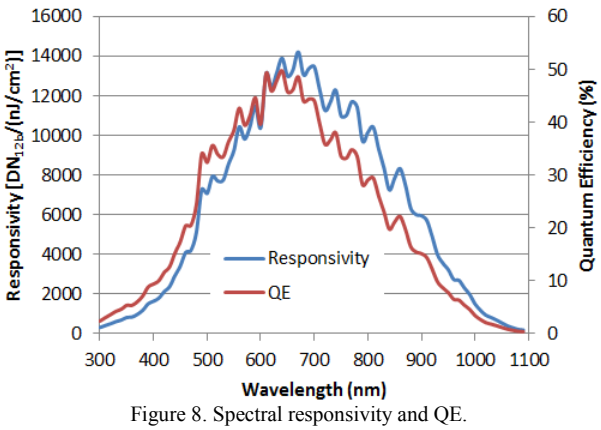

Figure 8. Spectral responsivity and QE.

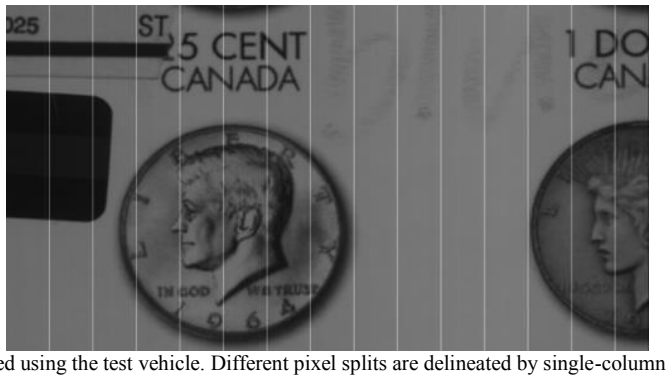

Figure 9. TDI drum image captured using the test vehicle. Different pixel splits are delineated by single-column gaps (vertical white strips in the image).

The test results are summarized and compared to the performance parameters of our proprietary CCD-TDI camera in TABLE I. The developed imager matches and/or outperforms the traditional CCD-TDI in several key performance parameters.

TABLE I. Performance comparison between the developed imager and the traditional CCD-TDI.

Parameters	Unit	Developed imager	Traditional CCD-TDI
CCD-CMOS monolithic integration	-	Yes	No
Pixel pitch	μm	5	5.2
Selectable TDI stages	Stages	64/128/192/256 (full)	
TDI scan direction	-	Bi-directional	
Maximum TDI scan rate	kHz	270	90
CTE per transfer	Fraction of 1	> 0.99999	> 0.99999
Full well capacity	Electrons	> 30,000	> 35,000
AB	×Saturation	Design for > ×100 (to be quantified)	×100
Dark current at 25°C	nA/cm^2	3.7	< 0.1
Non-linearity	%	< 2	< 2
Peak responsivity	$(DN_{12b})/(nJ/cm^2)$	14,000 at 670 nm	4,800 at 520 nm
Read noise	Electrons	12	30
Power consumption	Watt	2 for 4k resolution imager	40 for 12k resolution camera

V. Conclusion

We have developed the charge-coupled CMOS TDI imager using the custom CCD technology successfully integrated into a standard 0.18 μm CMOS technology. The ultra-compact imager with CCD pixels and CMOS peripheral circuits monolithically integrated demonstrates promising results such as low noise, high speed, very high responsivity and low power consumption for a variety of applications that the CCD-TDI imager has served traditionally.

References

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