

## **An imager with five 20000 x 15 pixel TDI CCDs for photogrammetry applications**

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### Introduction

Though CMOS imagers have widely taken over from CCDs, Charge Coupled Devices are still used in applications where the TDI (charge-domain time delay and integration) functionality is essential in achieving the required application performance. This paper presents a CCD imager with five TDIs on one chip, for use in high-end airborne photogrammetry applications. Each TDI array has 20016 x 15 pixels of 5.0 x 5.0  $\mu\text{m}^2$ . The vertical pitch between the five TDI arrays is 2.2 mm. The five TDI CCDs are used in combination with a beam splitter combined with external color filters to obtain blue, green (2x), red and near-infrared (NIR) information from the scene.

### Application Requirements

This CCD imager was developed in 2011-2012 based on the customer's requirements where the application and optical system dictated the pixel size, resolution, the number of TDI stages and the distance between the different TDI CCDs.

### CCD process and design basics

The CCD is manufactured using a n-channel CCD in a p-well on a n-type substrate to obtain buried-channel operation with anti-blooming [1]. Two layers of membrane transparent poly-silicon gates are strapped with metal-one (W). A second layer of metal (Al) is used for light shield and off-image interconnects [2]. The minimum litho dimensions are 0.35  $\mu\text{m}$ .

### Device Architecture

The overall CCD architecture is shown in Fig.1, and the detailed schematic of one TDI is shown in Fig.2. TDI2 (Gr1) and TD4 (R) are horizontally offset 2.5  $\mu\text{m}$  (half of the pixel pitch) compared to TDI1 (Gr), TDI3 (B) and TDI5 (NIR). Each TDI array has separate bonding pads for all register, amplifier control and output signals, located at the left and right side of each TDI. The control signals for the TDI image part are common for all five TDI arrays, and are located at the top and bottom of the total CCD imager. The readout can be done through either left or right side, or by split-read on both sides.

### Pixel Optimization

In a CCD with vertical anti-blooming, the collection depth is limited by the depth of the local potential minimum that defines the overflow barrier to the substrate. With shrinking pixels sizes, due to 3D effects, this results in a shift of the local potential minimum towards the surface. This reduces the QE, especially in the near infrared (750 - 900nm). We were able to increase the collection depth from 1.9 $\mu\text{m}$  to 2.3 $\mu\text{m}$  by skipping half of the p<sup>+</sup> channel stops between the columns without impacting the anti-blooming performance. Fig.3 shows the conventional pixel approach, while Fig. 4 shows the reduced channel stop concept. As the application has incident light angles not exceeding 10<sup>0</sup>, this asymmetry has hardly any impact on the optical performance of

the system. Fig.5 shows the results of 3D electrostatic simulations to optimize the pixel for charge capacity, collection depth and anti-blooming.

### Stage selection

To vary the integration time of the CCD, the number of TDI stages (CCD “lines” in static operation) that contribute to the final signal can be selected (1, 2, 4, 8 or 15). This selection is achieved by connecting the electrodes to different sets of metal-1 straps, and by reversing the transport direction of the non-selected groups of lines, towards the drain located above the imaging areas instead of towards the horizontal register. Fig. 6 shows a schematic of interconnect, with horizontally the four-phase polysilicon gates and vertically the metal straps. The yellow dots represent the contacts from straps to polysilicon.

### Interconnect Considerations

Special attention was paid to a very symmetrical design (left - right) for all output amplifier and horizontal register interconnects of the five TDI arrays. Also the routing in the package was optimized to avoid cross-talk.

### Stitching Design

As the size of the sensor exceeds the maximum stepper size in horizontal direction, the sensor is stitched by means of three different blocks: left edge (1x), center part (4x) and right edge (1x), as shown in Fig. 7. A detail of the left edge design is shown in Fig. 8.

### Performance

The performance of the CCD is summarized in Table 1. The linearity plot (Fig. 9) shows excellent performance up to 85% of saturation. The QE is show in Fig. 10, and the angular response is shown in Fig.11. Fig. 12 shows a picture taken with this CCD, and Fig. 13 shows the assembled device.

### Summary and Conclusions

The design and performance of a CCD imager with five 20016 x 15 pixel TDIs is presented, meeting all requirements for high-end airborne photogrammetry applications.

### References

- [1] “A 36x48mm<sup>2</sup> 48M-pixel CCD imager for professional DSC applications”, E.-J. Manoury et al., Proceedings IEDM 2008 (San Francisco, CA, 2008).
- [2] “A low dark current double membrane poly-Si FT-technology for 2/3 inch 6M pixel CCD imagers”, H. Peek et al., Proceedings IEDM 1999 (Washington DC, 2009).

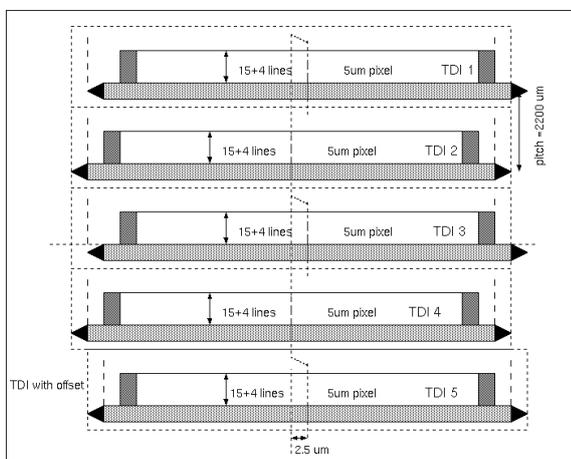


Fig.1. Schematic of imager with 5 TDI CCDs (aspect ratio not to scale)

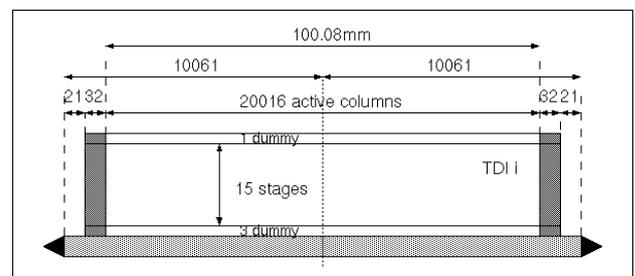


Fig.2. Schematic of one TDI CCD

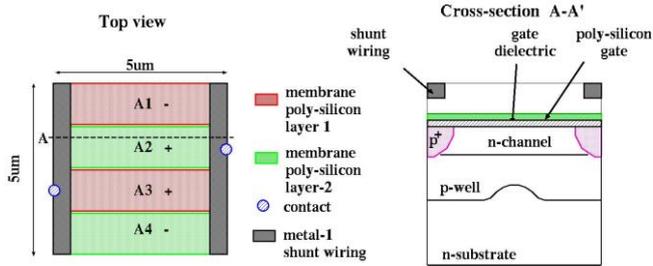


Fig.3. Conventional four-phase pixel with vertical anti-blooming.

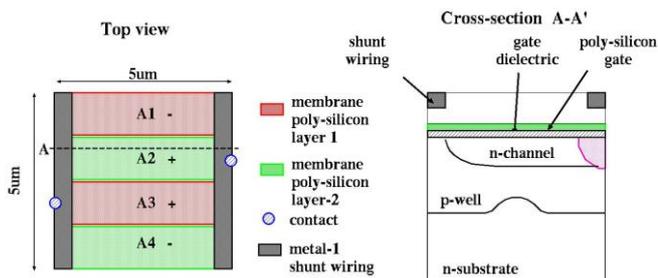


Fig.4. Pixel with reduced channel stops. The left-side channel stop is replaced by a 'no n-channel implant in p-well' isolation

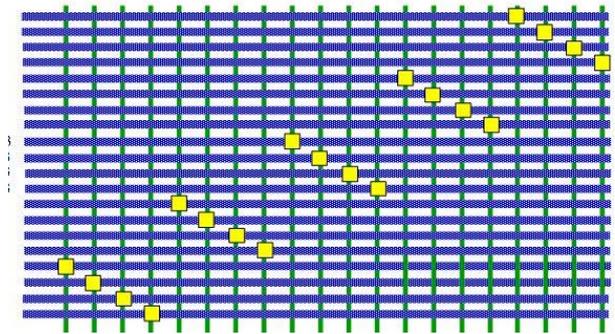


Fig.6. Schematic of interconnect concept in image area, allowing stage selection by reversing transport direction



Fig.7. Stitching blocks

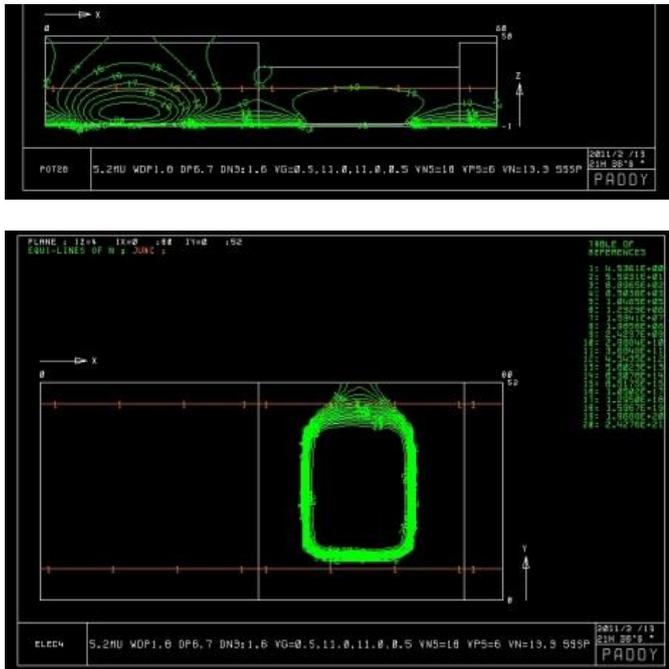


Fig.5. Simulation results of two adjacent pixels in transport direction, empty pixel (L) and full pixel (R).  
Top: potential distribution in transport direction  
Bottom: top view of charge distribution. Asymmetry can be clearly seen between lower pixel boundary (with channel stop implant) and upper boundary (without implant)

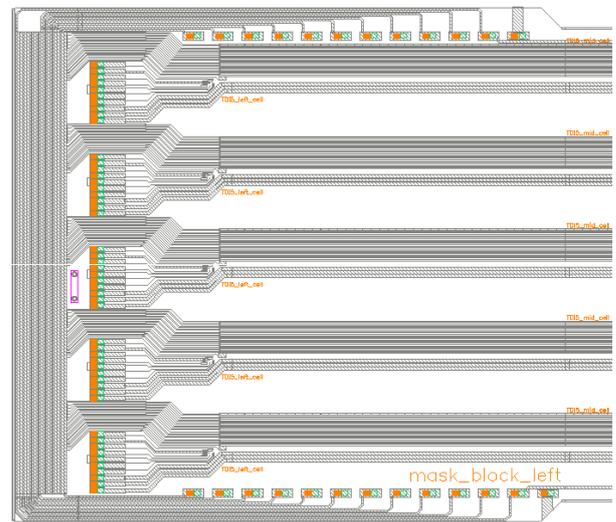


Fig.8. Details of left edge design

PARAMETER	TYPICAL	UNIT
Full well capacity (Qmax)	50000	e <sup>-</sup>
Linear full well capacity (Qlin)	42000	e <sup>-</sup>
Amplifier conversion gain	33	μV/e <sup>-</sup>
Maximum output voltage swing	1650	mV
Amplifier noise over full bandwidth after CDS	12	e <sup>-</sup>
Dynamic Range (at 22 MHz)	72.4	dB
Linear Dynamic Range (at 22 MHz)	70.9	dB
Overexposure handling	500	x Qmax
Horizontal Charge Transfer Efficiency	> 0.999995	-

Table 1. Performance Summary.

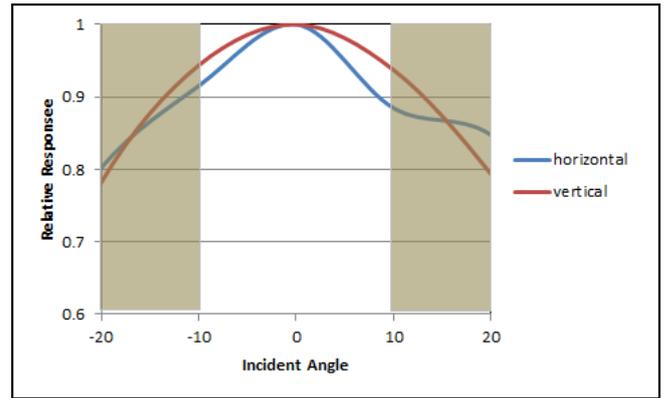


Fig. 11. Angular response for white light. Incident angles in application are limited to 10°.

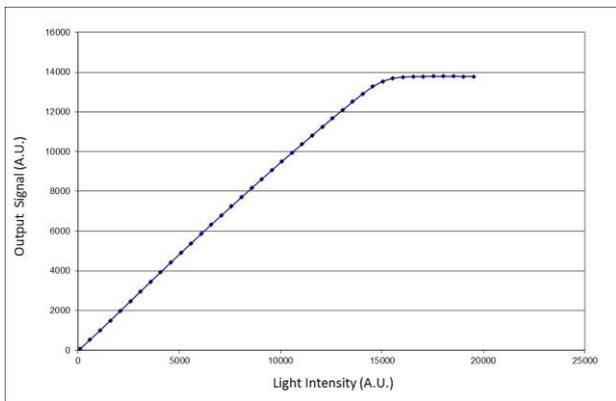


Fig.9. Linearity



Fig.12. Image obtained in application with aerial photogrammetry camera using CCD with 5 TDIs.

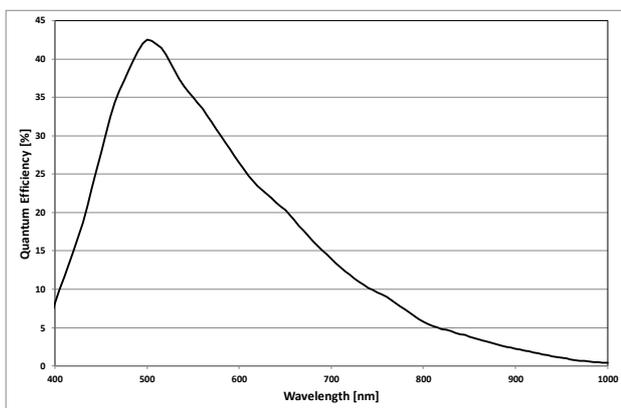


Fig.10. Quantum Efficiency



Fig.13. 5-TDI CCD in package.