Ultrafast signal processing readout front-end electronics in CMOS 40 nm technology for hybrid pixel detectors operating in Single Photon Counting mode

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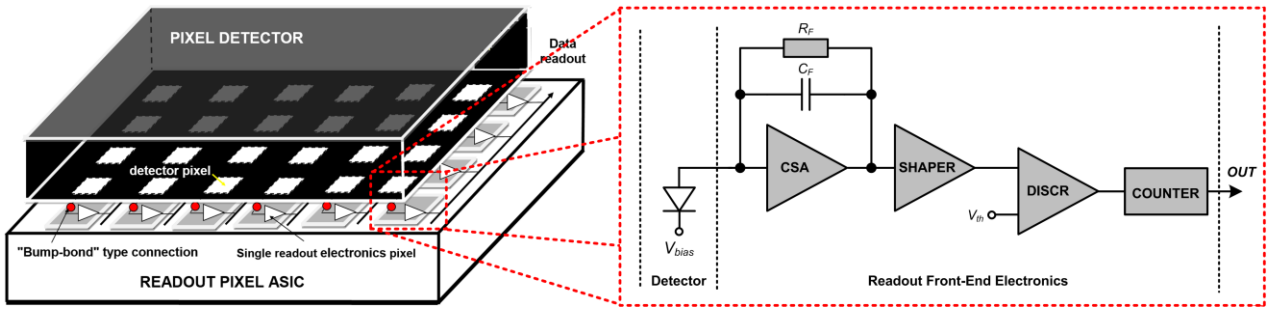
Abstract: This paper presents readout front-end electronics operated in the Single Photon Counting mode implemented in a CMOS 40 nm technology, which 10% dead time loss input rate parameter breaks the limit of 1×10^9 photons·mm^{-2}·s^{-1}. The prototype ASIC core is a matrix of 24 × 18 square pixels with a pitch of 100 µm. The single readout channel consists of a charge sensitive amplifier, a threshold setting block, a discriminator and a 24-bit counter with logic circuitry.

Keywords: X-ray imaging, high count-rate performance, single photon counting, pixel detectors

INTRODUCTION

More and more X-rays based imaging applications require to cope with high level of photons' flux, what taking into account low power and low noise requirements is a challenging task. In a hybrid pixel detector operating in the Single Photon Counting (SPC) mode each photon is processed independently by a separate readout front-end electronics (see Fig. 1a). The architecture of the single readout front-end electronics operated in the SPC mode usually consists of a Charge Sensitive Amplifier (CSA), a pulse shaping amplifier (SHAPER), a discriminator (DISCR) and a counter (see Fig. 1b). The main advantages of the SPC detectors are very high dynamic range (determined by counter depth), noiseless imaging (if a pulse amplitude is sufficiently high, properly set discriminator threshold cuts noise and counts only photon-related hits) and the possibility of counting photons only within a given energy windows (in systems with two or more discriminators). However, SPC systems are slower than integrating detectors (considering the number of photons which they can process per pixel per second).



(a) (b)

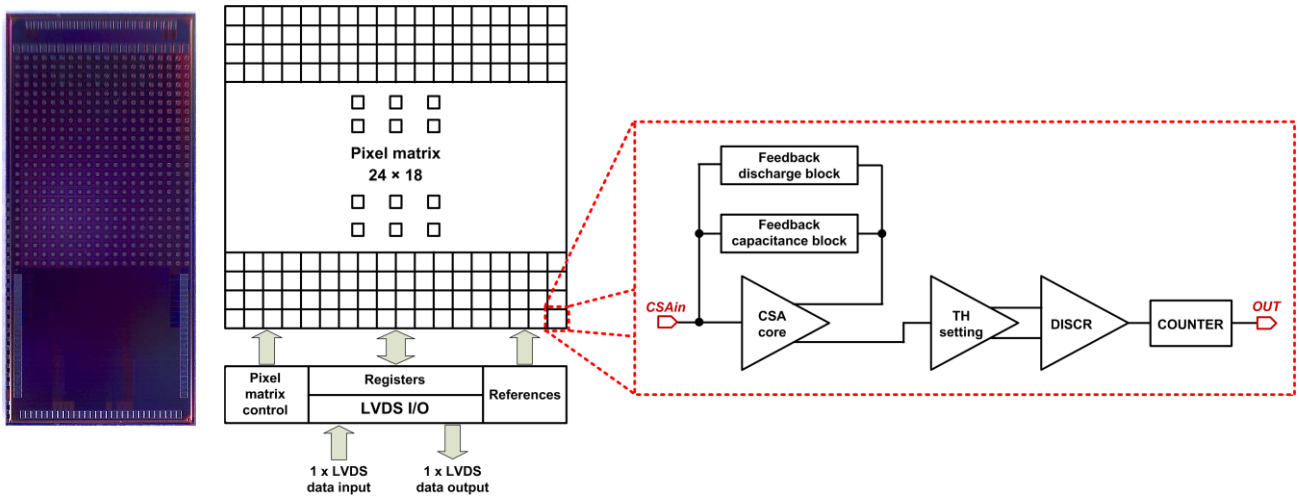
Fig. 1. (a) 2D hybrid pixel detector system – each detector pixel is connected to a separate readout channel, (b) Architecture of the readout front-end electronics operating in the Single Photon Counting mode.

THE PROTOTYPE ASIC

The prototype ASIC, implemented in CMOS 40 nm technology, contains 432 pixels (24 × 18 matrix) [1]. At the ASIC bottom part there are periphery (reference, control and communication) blocks – see Fig. 2a.

The single processing channel consists of an input stage (CSA), a threshold setting block (TH setting), a discriminator and a 24-bit counter with logic circuitry (see Fig. 2b). The CSA core is based on the folded cascode architecture. The CSA feedback capacitance block core is a set of 7 capacitors of value 1.2 fF to provide gain switching and gain correction functionalities. The CSA discharge block is based on the Krummenacher feedback structure. In opposite to the generic readout front-end electronics architecture in our solution there is no shaper stage (see Fig. 1b and Fig. 2b). The input signal is processed only by the CSA

stage, so the feedback discharge block not only discharges the CSA output pulse and compensates detector leakage current, but it also shapes the CSA output pulse.



(a) (b)

Fig. 2. (a) Photo and architecture of the prototype ASIC,
(b) Architecture of the presented readout front-end electronics analog part.

Depending on the CSA input transistor current I_{DM1} and the effective CSA feedback resistance R_F, the input stage operates in the following mode:
- *FAST* mode: $I_{DM1} \approx 20$ µA (CSA's core $GBW \approx 5.3$ GHz) and R_F of the order of MΩ,
- *FAST_HC* (*High Current*) mode: $I_{DM1} \approx 60$ µA (CSA's core $GBW \approx 8.4$ GHz) and R_F of the order of MΩ.

Threshold setting block provides not only threshold setting functionality, but also the correction of the effective threshold level at the discriminator input to reduce the effects of mismatch.

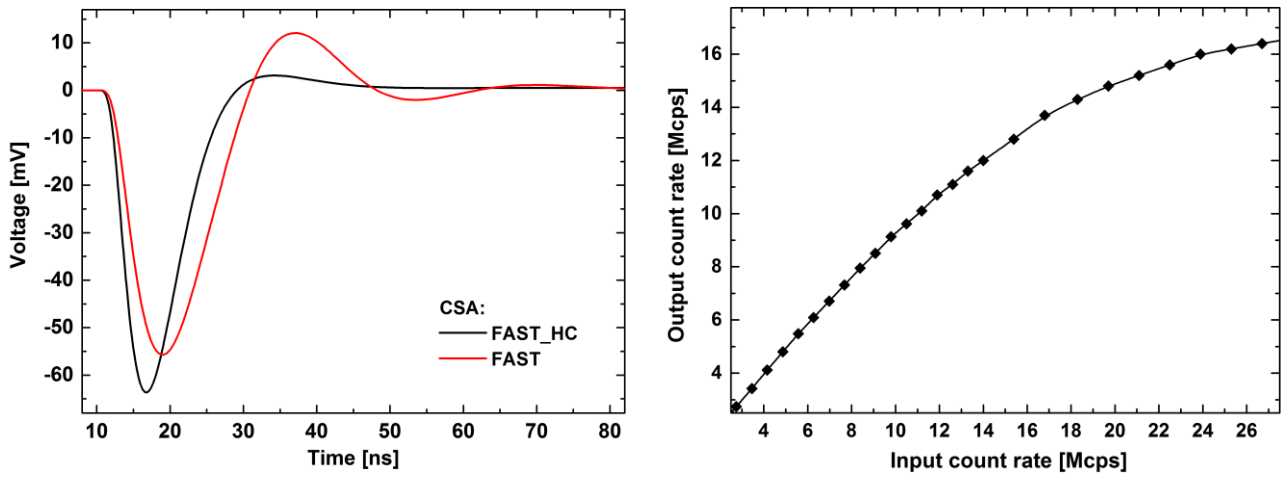
The single pixel size is 100 µm × 100 µm including other test structures. The essential analog part occupies around 20 µm × 70 µm of silicon area, while the digital circuitry area is around 20 µm × 50 µm, meaning that a single pixel would occupy the silicon area of 50 µm × 50 µm.

SIMULATIONS AND MEASUREMENTS RESULTS

The post-layout simulated CSA output waveforms for input charge $q_{in} = 2200$ e$^-$ for the CSA operating in the *FAST* and *FAST_HC* modes are presented in Fig. 3a. The CSA feedback discharge time constant $\tau_F = R_F \cdot C_F$ values for both cases are approximately 4 ns, whereas the CSA input transistor transconductance g_{m1} values are: $g_{m1} = 0.38$ mA/V for the *FAST* and $g_{m1} = 0.84$ mA/V for the *FAST_HC* mode. The CSA output pulse rise time constant $\tau_R \propto 1/g_{m1}$, what implies that increasing the g_{m1} value means decreasing the CSA output pulse rise time constant τ_R. Additionally, higher transconductance g_{m1} value implies lower noise *ENC* value. The post-layout simulated noise performance for the *FAST* and *FAST_HC* modes are: *ENC* = 158 e$^-$ rms and *ENC* = 104 e$^-$ rms respectively.

The CSA output pulse shape (its amplitude and noise performance) can be controlled by changing the ratio τ_F/τ_R [2]. From simplified theoretical point of view, when the ratio $\tau_F/\tau_R > 4$ the output pulse is a combination of two exponential functions and can be considered as an unipolar pulse shaping – see the *FAST_HC* mode waveform in Fig. 3a. Otherwise, the output pulse contains a sinusoidal term multiplied by an exponential one, but in this case to prevent from oscillation in a pulse response the ratio $\tau_F/\tau_R > 3$ – see the *FAST* mode waveform in Fig. 3a. When the CSA output pulse response has only one undershoot it can be approximately considered as a bipolar pulse shaping.

The measurement tests were performed with the IC bump bonded to a 320 µm thick silicon pixel detector biased up to 150 V. During measurements 6 rows of pixels were illuminated by 8 keV X-rays source. The measured count rate performance of the CSA operating in the *FAST_HC* mode is presented in Fig. 3b. The average value of measured noise *ENC* and 10% dead time loss input rate N_{IN} parameters are presented in Tab. 1 (see two rightmost columns). The 10% dead time loss input rate N_{IN} is defined as an input rate N_{IN} at which the output count rate $N_{OUT} = 0.9 \cdot N_{IN}$. When the 10% dead time loss input rate parameter is combined with the single readout pixel area, its unit is expressed as photons·mm^{-2}·s^{-1}.



(a) (b)

Fig. 3. (a) The post-layout simulated CSA output waveforms for the CSA in the FAST and FAST_HC modes, (b) Measured count rate performance for the CSA in the FAST_HC mode.

To conclude the measurement results, it is possible for the CSA in the *FAST* mode to operate as fast as in the *FAST_HC* mode, however at the price of higher noise *ENC* value. The measurements show that the described readout front-end electronics is according to the authors knowledge currently the fastest SPC based solution (5.5 times faster than the fastest UFXC32k IC reported so far - see Tab. 1), while the power and noise are at the acceptable level. The presented readout front-end electronics' 10% dead time loss input rate parameter breaks the limit of 1×10^9 photons·mm^{-2}·s^{-1}. The presented parameter's values were calculated based on the pixel size 100 µm × 100 µm (with many test structures). Having in mind, that a single pixel with blocks needed for only fast signal processing would occupy the silicon area of 50 µm × 50 µm, it additionally would increase substantially the value of the 10% dead time loss input rate parameter.

Table 1. Comparison of counting chips in submicron CMOS technologies

Chip [ref]	Medipix 3RX [3, 4, 5]	PILATUS3 [6]	PXD18k [7]	Eiger [8]	UFXC32k [9]	This work	
						FAST_HC	FAST
Process	130 nm	250 nm	180 nm	250 nm	130 nm	40 nm	
Pixel size [µm^2]	55×55	172×172	100×100	75×75	75×75	100×100	
Power/pix. [µW]	9	15*	23	–	26	103	46
ENC [e$^-$ rms]	80	–	168	175	235	185	212
10% dead time loss input rate # [photons mm^{-2} s^{-1}]	0.87×10^8	0.53×10^8	0.61×10^8	1.46×10^8	2.20×10^8	1.22×10^9	1.22×10^9

* static PWR consumption for minimum dead time τ_p of the front-end electronics .

calculated using minimum dead time and assuming $N_{OUT}/N_{IN} = 0.9$ according to the formula: $N_{OUT} = N_{IN} \cdot \mathrm{EXP}(-N_{IN} \cdot \tau_p)$.

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