Two-tier Geiger-mode avalanche detector for charged particle imaging

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Abstract

In this contribution, we present the first demonstration of a new type of silicon sensor for the direct detection of charged particles. The proposed device, based on 3D-integrated Geiger-mode avalanche diodes, features early signal digitization, sub-nanosecond timing and low material budget. The Dark Count Rate is dramatically reduced thanks to the coincidence between two vertically-integrated layers. A preliminary demonstration of sensor operation in the dark and in the presence of charged particles is presented.

Introduction

Sensors based on Single Photon Avalanche Diodes (SPAD) are currently expanding from niche markets to consumer electronics thanks to their possibility of being CMOS integrated. Their picosecond timing resolution and intrinsic amplification characteristics are the key to low-power fast optical sensors with excellent Signal to Noise ratio [1]. Research on new architectures and 3D integration possibilities are making them more and more applicable in a variety of optical sensing applications [2].

In this work, we demonstrate a CMOS-integrated sensor based on Geiger-mode avalanche diodes for the direct detection of charged particles. The proposed device, formed by two vertically-aligned pixelated detectors, exploits the coincidence between two simultaneous avalanche events to discriminate between particle-triggered detections and dark counts (Figure 1) [3]. This approach offers several advantages in applications requiring low material budget and fine detector segmentation as, for instance, for tracking and vertex reconstruction in particle physics experiments and charged particle imaging in medicine and biology.

Sensor design

A two-tier sensor assembly was designed and fabricated in a commercial 0.15µm CMOS process. The sensor consists of a 48x16 pixel array, and includes avalanche diodes of different sizes and types [4]. Each pixel, having a 50µm x 75µm area, includes detectors and electronics on both layers, with the top-layer signal transmitted to the bottom layer using a vertical interconnection per pixel (Figure 2). Bump bonding technique using 12-µm solder bumps was adopted for the vertical integration. The detectors were covered with a metal shield to avoid inter-layer optical cross-talk.

The schematic diagram of a 2-level pixel is shown in Figure 3. In the pixel, the detectors are passively quenched and their output signals are digitized by means of a low-threshold comparator. The resulting pulses are shortened by a programmable-length monostable circuit. The pixels can be independently enabled or disabled with an arbitrary pattern, defined by a configuration register. The output of the monostable in the top half-pixel feeds a coincidence detector located in the bottom layer, and the coincidence output is stored in a 1-bit memory. Data can be transferred in parallel to an output register for the readout. The monostable outputs are also fed to a row-wise OR gate, and a circuit for mapping the coincidence between arbitrarily-selected rows is present (Figure 4). These features were included to map the dark count rate (DCR) and crosstalk probability between different pixels.

CHARACTERIZATION

A micrograph of the bottom chip is shown in Figure 5, with a close-up of unshielded pixels having different active area. A concept view of the vertically-integrated sensor is illustrated in Figures 6. The top and bottom tier are connected through SnAg soldering bumps, while the bottom layer is connected to the package using standard wire bonding.

A first characterization was conducted on the single layers to evaluate the performance of the SPADs in terms of correlated and uncorrelated noise. Dark Count Rate (DCR) statistics was acquired at different temperatures, enabling one pixel at a time to exclude the effects of optical cross talk. A median DCR of 3 kHz was measured for the largest detectors, having 43µm x 45µm active area, at an excess voltage V_{EX} = 3.3V and T=20°C (Figure 7). Figure 8 compares the DCR distribution obtained by activating one SPAD at a time and with all the pixels active at the same time. The observed difference is due to optical cross-talk. This effect was found to strongly affect the measured DCR at large excess voltages, especially for low-DCR detectors [5].

The coincidence DCR distribution measured on the 3D-integrated sensors is shown in Figure 9 for three different settings of the monostable circuit. By setting a pulse width of 0.75ns, the coincidence DCR is lower than 100mHz for 80% of the pixels. Functional tests with a ^{90}Sr beta source and a test beam with Minimum Ionizing Particles have been carried out. Preliminary results are shown in Figures 10 and 11, and data analysis and Monte Carlo simulations are under way to obtain a thorough understanding of all the factors affecting sensor efficiency.

CONCLUSION

In this work, we have demonstrated the feasibility of a two-tier charged-particle sensor based on Geiger-mode avalanche diodes. This approach offers a unique combination of low-material budget, sub-nanosecond timing, and low power operation, that can be exploited in medical and fundamental physics research applications.

ACKNOWLEDGMENT

The research activity presented in this contribution has been carried out in the framework of the APiX2 experiment funded by Istituto Nazionale di Fisica Nucleare (INFN), CSN5.

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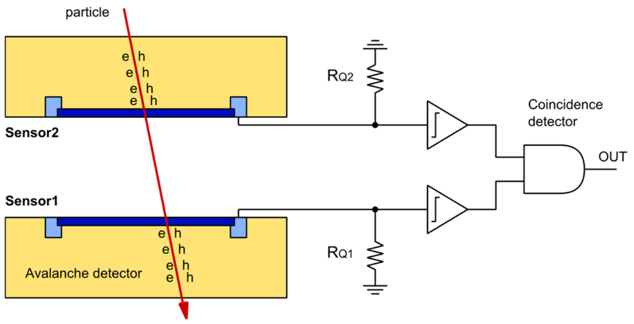

Figure 1. Concept of coincidence detection.

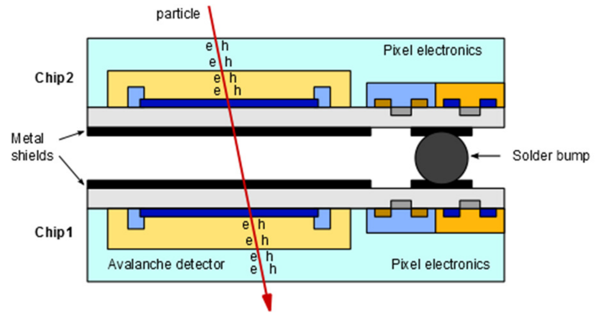

Figure 2. Pixel simplified cross-section.

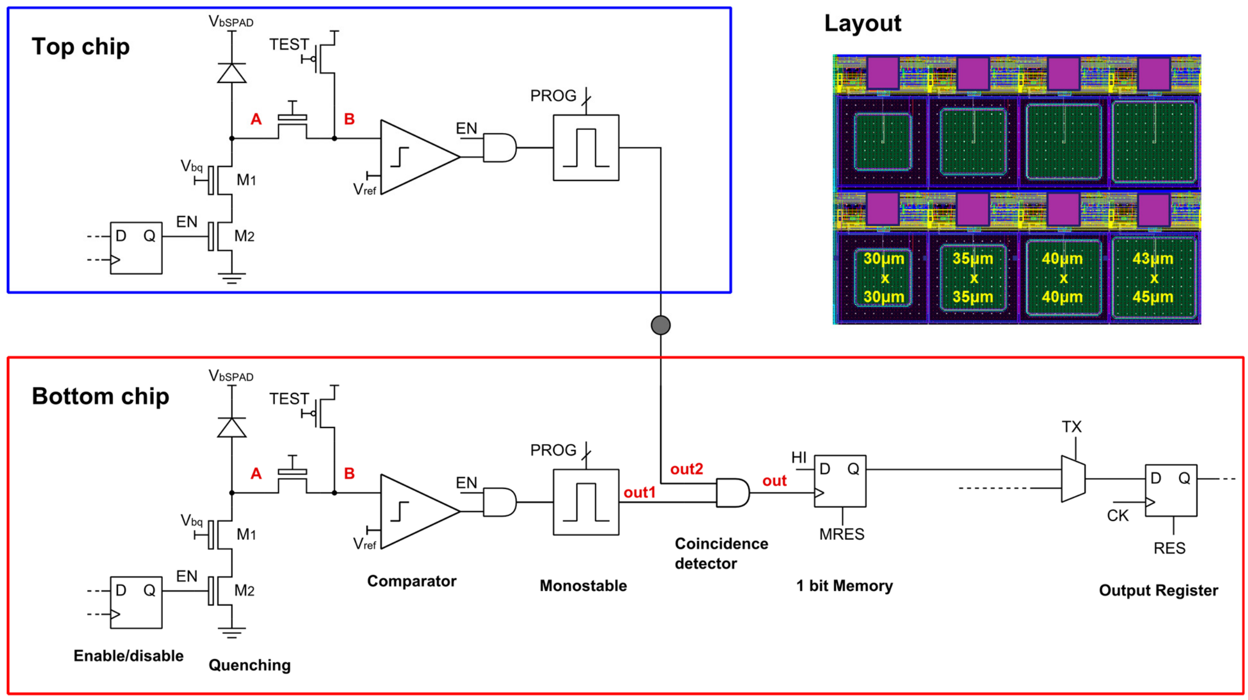

Figure 3. Pixel schematic diagram and layout of 8 pixels with different active areas.

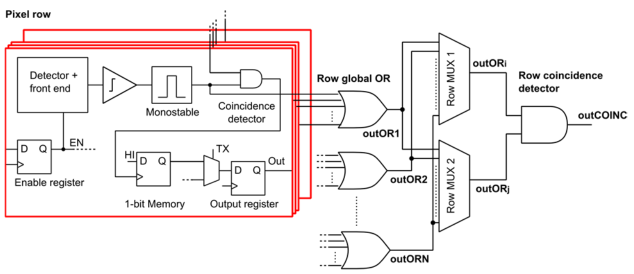

Figure 4. Peripheral circuitry for row coincidence detection.

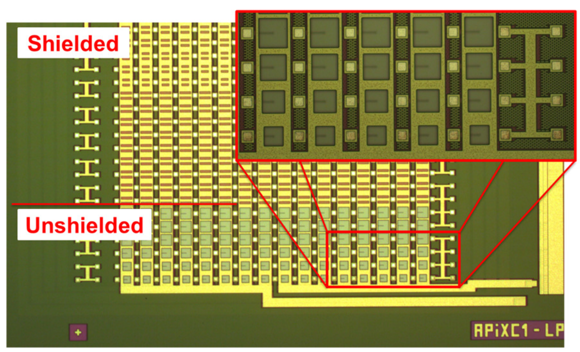

Figure 5. Bottom chip micrograph.

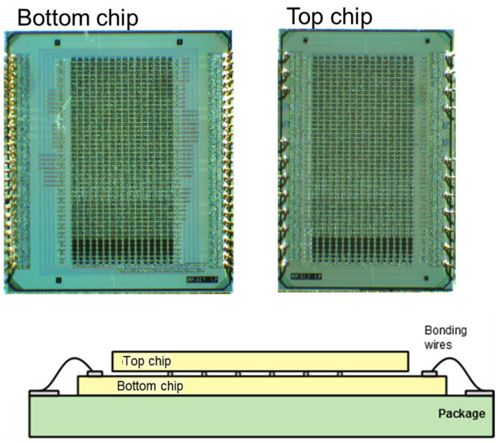

Figure 6. Chip micrographs and concept drawing of the vertically-integrated assembly.

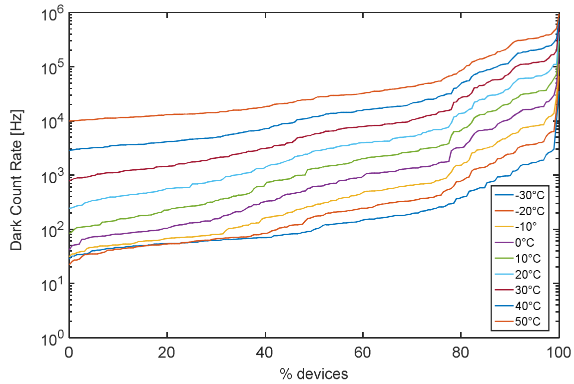

Figure 7. DCR distribution at different temperatures for the large devices (43µm x 45µm active area) at V_{EX}=3.3V.

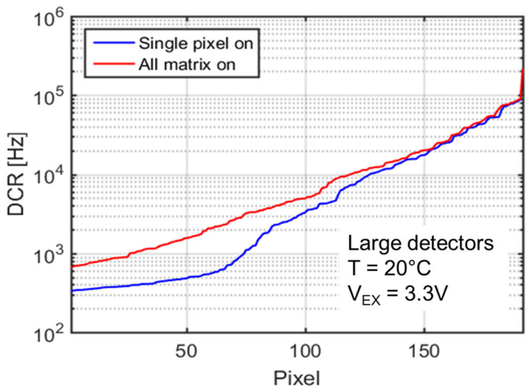

Figure 8. DCR distribution measured enabling one pixel at a time and with all the pixels enabled simultaneously.

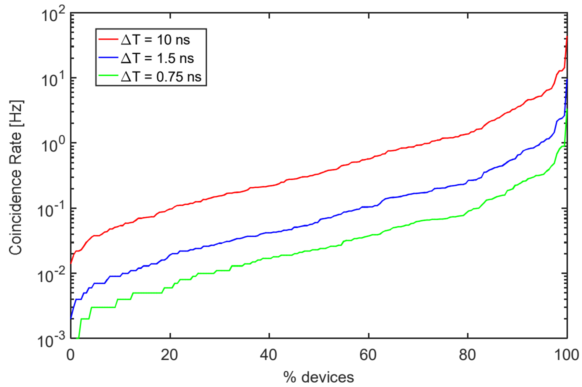

Figure 9. DCR in coincidence with three different settings of the monostable circuit at V_{EX}=1V and T=20°C.

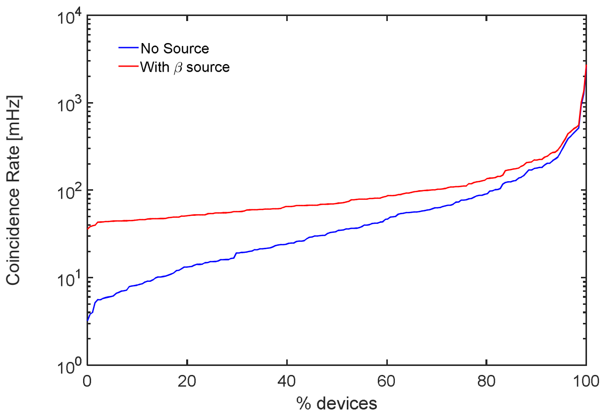

Figure 10. Distribution of coincidence DCR and count rate in the presence of a 37kBq ^{90}Sr β radioactive source at V_{EX}=2V and T=5°C.

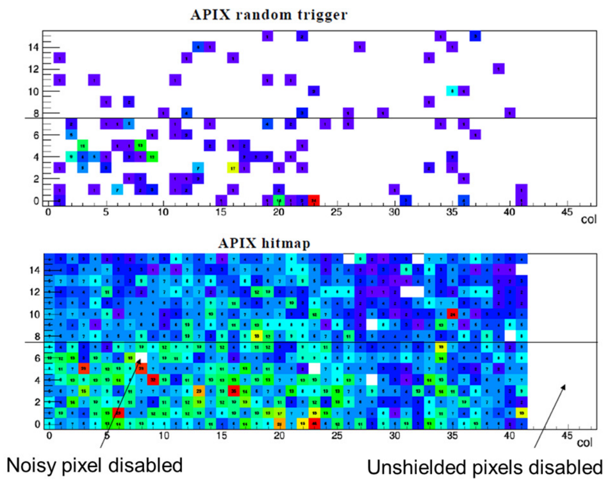

Figure 11. Top: dark count rate map. Bottom: hit map acquired during a test beam with positrons and pions at CERN.