Column-Parallel Dynamic TDC Reallocation in SPAD Sensor Module Fabricated in 180nm CMOS for Near Infrared Optical Tomography

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Abstract

A major problem for optical biomedical imaging methods, e.g. near-infrared optical tomography (NIROT), using time resolved SPAD sensors is a slow acquisition time, resulting in motion artefacts and decreased patient comfort. We present a new SPAD sensor module optimised for the NIROT application. Dynamic TDC reallocation is employed to reduce the die area occupied by timing circuitry whilst also minimising the probability of photon pileup. High pixel PDE is achieved with a wide spectral range SPAD and cascoded passive quenching circuit. The sensor is fabricated in a 180nm CMOS process, enabling an image acquisition time in the NIROT application of 3.8 seconds per source and wavelength pair.

Introduction

Ischaemic brain injury, a lack of oxygen in the brain, is a major cause of long term disability and death for babies born prematurely. A promising method for determining the oxygenation of the brain is near infrared optical tomography (NIROT), where the tissue under study is illuminated by light in the wavelength range of 650-900 nm. We are working on a new approach to NIROT using single-photon avalanche diode (SPAD) based image sensors in a contactless setup [1], shown in Figure 1. In comparison to conventional methods, this approach has the advantage of a greatly increased number of detectors, thereby promising an improved spatial resolution. A critical performance parameter in such systems is the image acquisition time. A shorter acquisition time reduces the impact of motion artefacts and improves patient comfort. For the image sensor design, this implies a high degree of parallelism is required. Typically, this means placing a TDC in every pixel. In frontside-illuminated implementations, this results in low fill factor and a photon throughput limited by the need to readout null events. In this paper, we present a SPAD image sensor, Figure 4, designed in a 180 nm CMOS process, optimised for high speed image acquisition in the NIROT application. High speed is ensured thanks to high levels of parallelism whilst high PDE is achieved with a wide spectral range SPAD [2], compact cascoded quenching circuit and extensive sharing of timing resources.

Event Driven TDC Reallocation

To maximise the sensor fill-factor and photon throughput, we use a new event-driven TDC reallocation architecture. As in [3], a large number of pixels can trigger any TDC in a bank, however, in our architecture it is also possible to capture the pixel address. The outputs of each pixel in a column are connected to a set of bus lines, which are each pulled up to V_{DD} using a PMOS transistor, Figure 3c. Upon the arrival of a photon, the pixel pulls down the timing line and a unique combination of 7 address lines. At the bottom of each pixel column, there is a series of 4 address latch and time-to-digital converter (TDC) circuits connected in a daisy chain. Upon the detection of a photon, the pixel address is captured by an address latch, whilst the timing line triggers the ring-oscillator (RO) TDC, Figure 5, which has a tunable least significant bit (LSB) controllable from off-chip, Figure 8. Once the address is latched the next slice in the chain is activated with LC_FLAG, Figure 6. At the end of each cycle, each slice which received a photon asserts the LC_RST signal,

resetting the preceding slice. Thus, a maximum of 3 photons per column are detected per cycle. Output data is read into a serializer via a latch selector block and tri-state bus, Figure 3d. Thus, no power is dissipated communicating null events, where no photon arrives, which is typically the case for TDC in-pixel architectures [4,5]. Each column has a dedicated GPIO for serial data transmission, maximising photon throughput and minimizing the image acquisition time in NIROT.

High-PDE Pixel

High sensitivity at NIR wavelengths is achieved with a low DCR SPAD with a wide spectral response [2]. A PDP of greater than 10% at 800 nm can be achieved when biasing with excess bias voltages greater than 5 V, Figure 2. To improve the pixel PDE and timing performance, we use a cascoded quenching scheme, Figure 3b, implemented with 3.3 V transistors, which allows the SPAD to be operated at excess bias voltages up to 5.2 V without exceeding the 3.6 V reliability limit across the gate-source, gate-drain and drain-source of any device, see Figure 7. Since this technique uses only transistors to increase the excess bias, the layout is very dense, achieving a fill factor of 28% with a pixel pitch of 28.5 µm × 28.5 µm.

Towards High Speed, High Resolution NIROT

The sensor was implemented in an array of 32 × 32 pixels with a total of 128 TDCs. With 32 output pads operating at 160 Mb/s, the maximum photon rate will be 269 Mphotons/s, whilst consuming less than 1.2 W of power. The sensor will be used in a NIROT setup consisting of an 80 MHz super continuum laser (Nkt Photonics) and acousto-optic tunable filter, enabling time-resolved measurements at multiple wavelengths. Assuming 10^6 photons are required per pixel, a measurement for each source and wavelength pair (a clinical system could use 16 sources and 4 wavelengths) will take 3.8 seconds for all 1024 pixels at maximum speed, thus enabling measurements on human subjects.

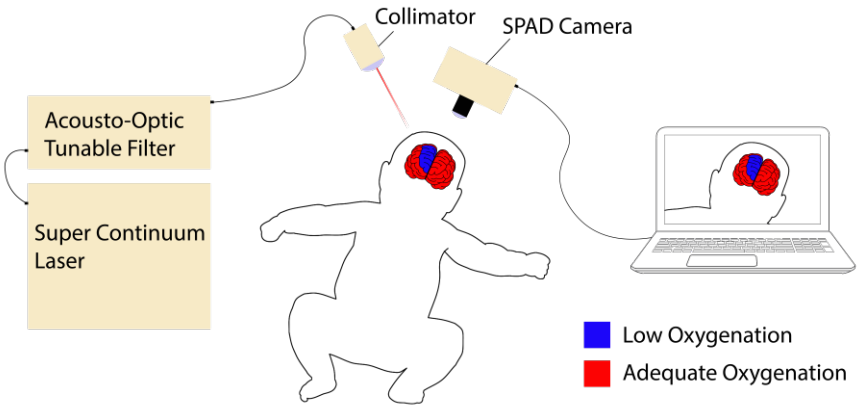

Figure 1. Contactless NIROT using a SPAD camera. The acousto-optic tunable filter selects a narrow wavelength band from the super continuum laser, allowing multiple wavelength measurements.

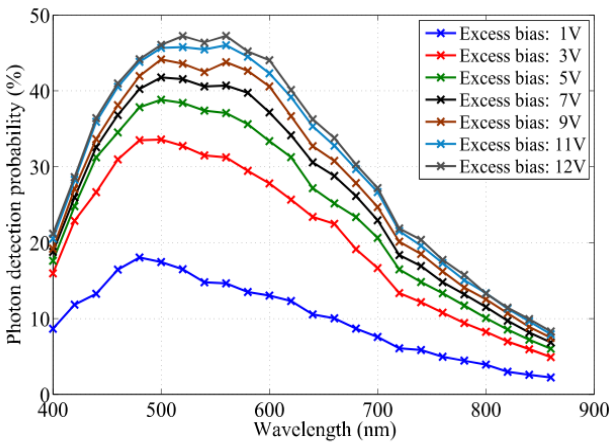

Figure 2. Wide spectral range SPAD PDP [2]

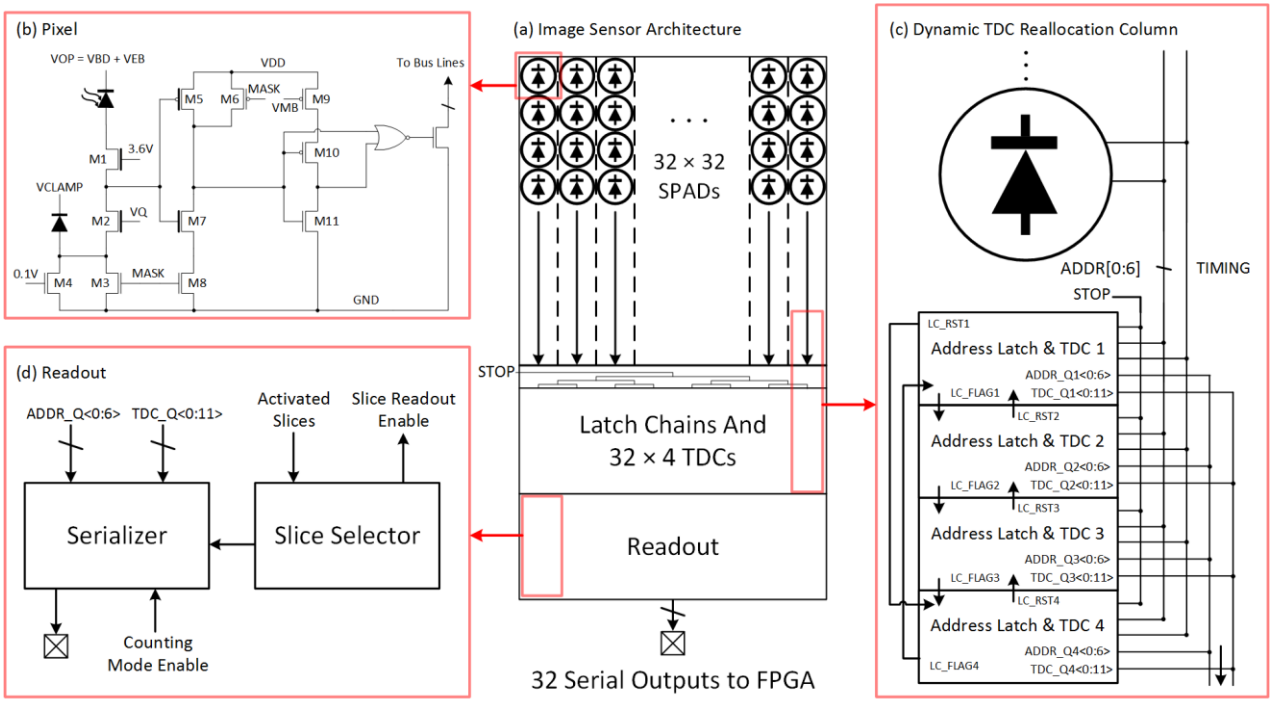

Figure 3. (a) Event-driven image sensor architecture, (b) High PDE cascoded quenching pixel, (c) Dynamic TDC allocation column with daisychained address latch and TDC blocks (d) Time-of-flight readout with counting mode to transmit only address data.

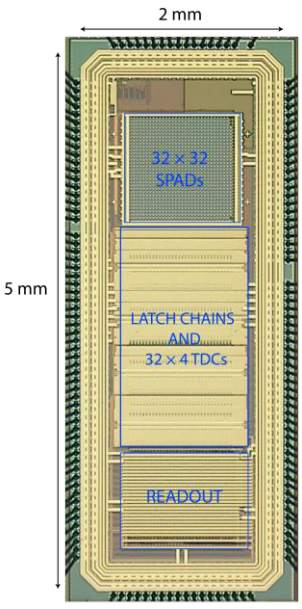

Figure 4. Chip micrograph

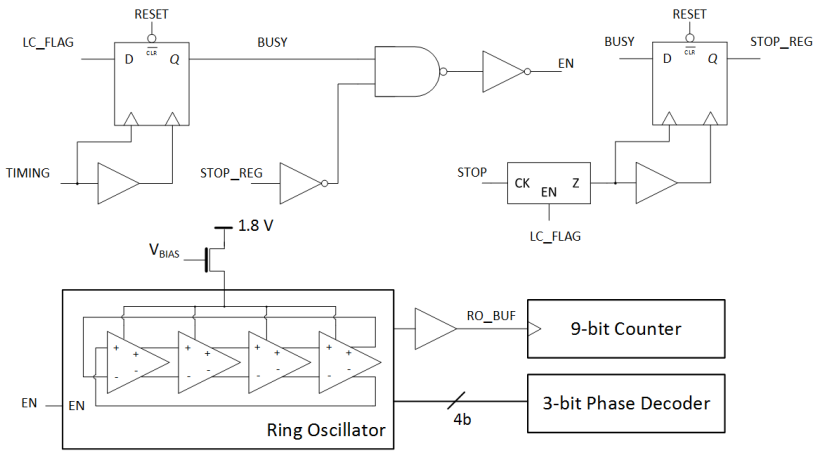

Figure 5. RO-TDC schematic, STOP signal is gated by flag to reduce static power consumption. Ring oscillator frequency is tuned with the gate bias V_{BIAS} of a thick oxide transistor to increase frequency range. PVT compensation can be implemented off chip via an on-chip replica RO.

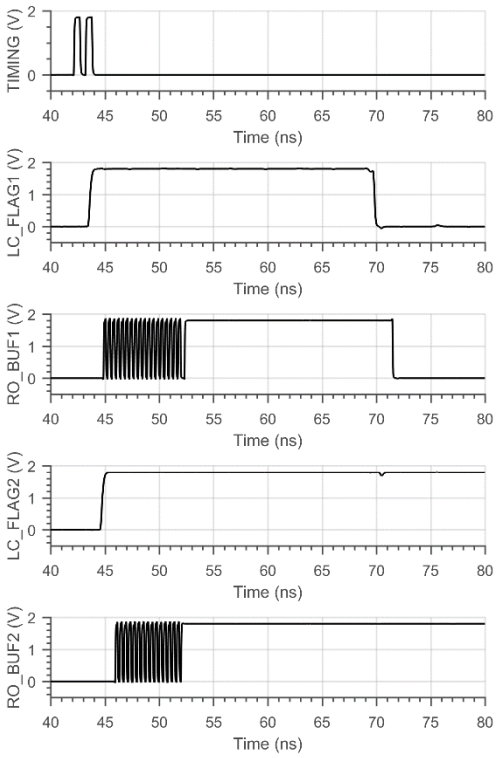

Figure 6. Post-layout simulation of TDC sharing column at 25°C. Two photons detected 1 ns apart, LC_FLAG signal activates next address latch and TDC slice. Timing activates RO-TDC. Address latch and TDC slice 1 reset by slice 2 after next clock (not shown) edge.

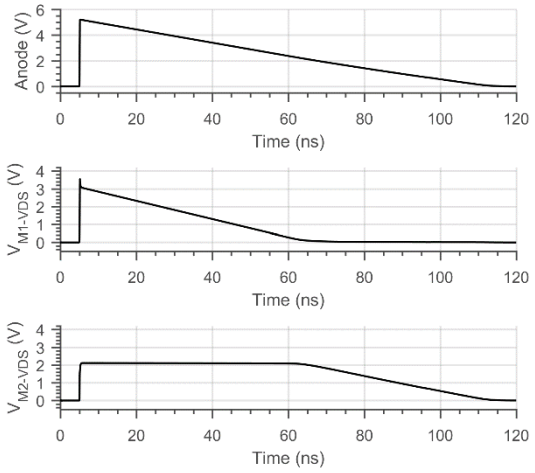

Figure 7. Pixel simulation of cascode quenching. The drain-source voltages (V_{DS}) of M_1 and M_2 are limited below 3.6 V at excess bias voltages up to 5.2 V.

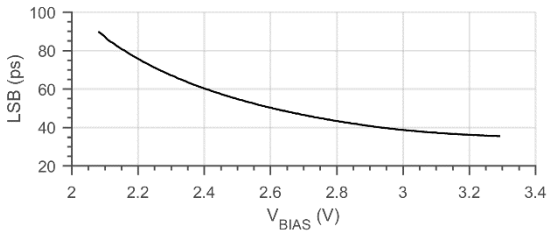

Figure 8. Tuning characteristic of RO with control voltage, V_{BIAS}, to set TDC LSB. Post-layout simulation in typical corner at 25°C.

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