Investigations on cryogenic operation of Pinned photodiode pixels

Philippe Martin-Gonthier, Pierre Magnan, Olivier Marcelot
ISAE-SUPAERO, Université de Toulouse, Toulouse, France
philippe.martin-gonthier@isae.fr, Phone: +33 5 6133 8369

***Abstract*— With the motivation of reducing ultimately the dark current of CMOS pinned photodiode (PPD) pixels to a negligible level, this work addresses some of the potential issues of operating PPD based pixels at cryogenic temperature. This temperature range, involving changes on several semiconductor parameters, does impact both the PPD itself but also the MOS devices of the pixel, leading to several modifications of characteristics which are reported and, for some, simulated.**

I. Introduction

For several scientific applications such ground or space based astronomy [1]-[3], despite the CMOS image sensors impressively low achievable readout noise and the improvements of their dark current figure, there is still a need for reducing further the dark current noise by operating the sensor to low and even cryogenic temperature (as it has been the case for the best CCD sensors). This will bring it to negligible level compared to readout noise even for long exposures. As can be seen in Figure 1, dark current measurements have been done at low temperatures using an image sensor fabricated in a CIS 0.18µm technology with a 7µm PPD pixel pitch. A very low dark current around 2.10^{-3} e/s is achieved at 200K. Much lower and even negligible values can be expected by reducing further the operational temperature (toward the 80K -100K range).

However, the behavior of modern CMOS imaging sensor based on Pinned Photodiode down to cryogenic temperature has not been investigated up to now. Operation of CMOS devices in the cryogenic temperature range does affect many semi-conductor mechanisms and parameters [4]: bandgap narrowing (slightly reducing the cut-off wavelength), increase of drift velocities and carrier mobilities, but also the incomplete ionization of doping impurities.

In this work we address some of the potential issues of PPD based pixels at such operational conditions, the first one being the pinning voltage variation at low temperature. By comparing measured pinning voltage at low temperature with TCAD simulation, an enhanced TCAD model is setup to provide an acceptable correlation between simulations and measurements. The electrostatic conditions in PPD and transfer gate area are then simulated in order to analyze the charge transfer conditions in the cryogenic temperature range. Finally, the transfer function of the readout chain at low and cryogenic temperature is also analyzed through measurements based on simple image sensor analog readout chain and MOSFET devices.

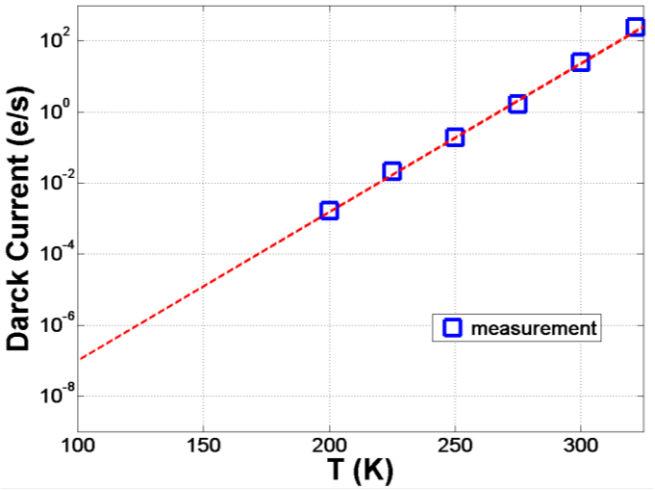

Figure 1: Dark current plot showing a strong decrease with very low temperature (PPD pixel with 7µm pitch in CIS 0.18µm technology)

II. Cryogenic Operation Impact on Pinning Voltage

JFET-like structures implemented on a CIS 0.18µm process with various dimensions of width W (from 0.6µm to 10µm) and length L (from 10µm to 30µm) have been used to extract pinning voltage by the square root method described in [5].

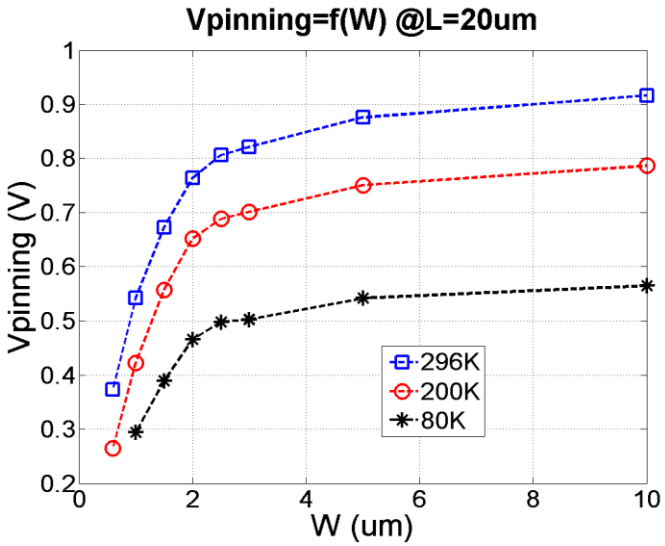

Figure 2: Measured Vpinning evolution vs W sizes and L=20um for 3 different temperatures

These structures have been placed in a dewar filled with liquid nitrogen. I-V measurements were done with a Keithley 4200 Semiconductor Characterization System. The measurement setup is shown Figure 3.

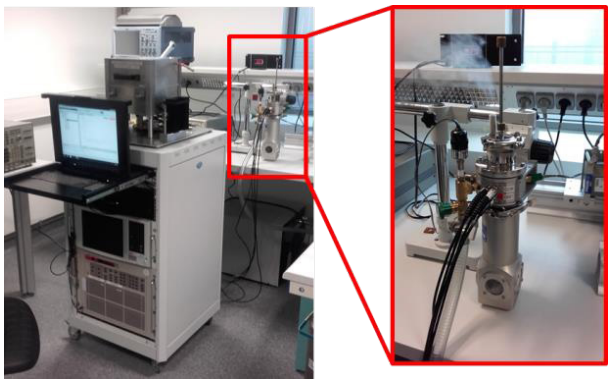

Figure 3: Cryogenic measurement setup including Keithley 4200 Semiconductor Characterization System for basic devices (MOST, PPD)

Pinning voltage measurements, reported in Figure 2 for various JFET-like structure sizes and three temperatures, clearly demonstrate a significant reduction of the pinning voltage at low temperature which can impact severely its FWC and modify charge transfer conditions.

A detailed analysis of the pinning voltage along temperature is depicted in Figure 4 for three width values.

For temperatures above 200K, the pinning voltage linear decrease follows equation (1), as demonstrated in [6], where ε_{Si} is the Si permittivity, W_{PPD} is the depth of buried channel, and N_{PPD} is the doping concentrations of the PPD buried channel implant. V_{bi} corresponds to the built-in voltage of the upper junction, which depends on the intrinsic concentration n_i, N_{PPD} and the pinning implant doping concentration.

$$V_{pin}(T) = \frac{qN_{PPD}W_{PPD}^2}{2\epsilon_{Si}} - V_{bi}(T) \qquad (1)$$

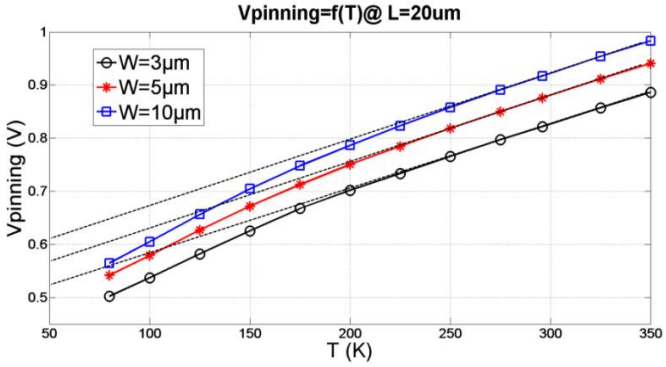

Figure 4: Measured Vpinning evolution vs temperature for 3 different W sizes and L=20um

In this temperature range, N_{PPD} is nearly constant, all impurities being considered as ionized.

Below 200K, the pinning voltage evolution departs significantly from the linear trend, with a reduction emphasized below 150K. It is due to the incomplete ionization of doping impurities, described in Figure 5 giving the fraction of ionized impurities along temperature, which modifies the electrostatic conditions of the pinned photodiode junctions, thus making its fully depleted condition very sensitive to low temperature.

TCAD simulations, shown in Figure 6 performed with standard models, i.e. without the incomplete ionization phenomenon taken into account, predict, as equation (1), a

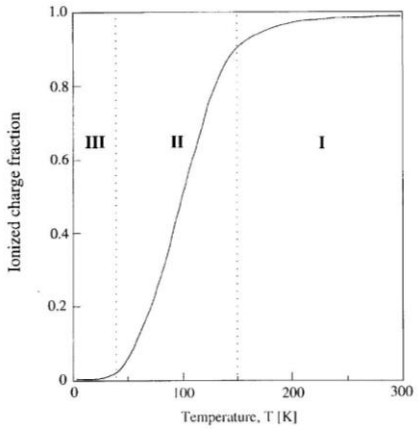

Figure 5: Ionized charge fraction vs Temperature from [4]

continuous linear evolution while decreasing temperature and so appear to be useless in helping in the analysis of the low temperature behavior.

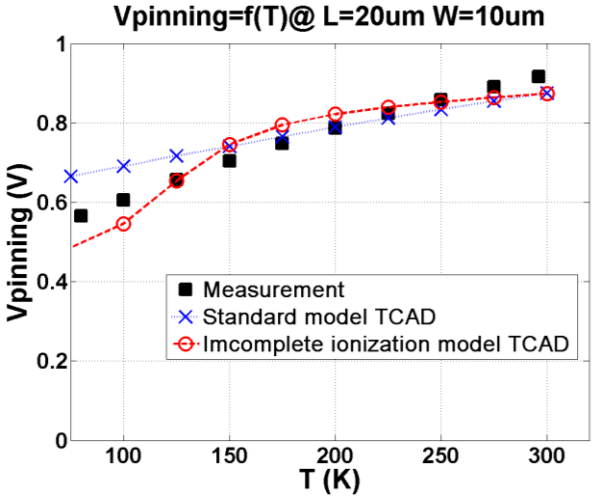

Figure 6: Vpinning evolution vs Temperature from measurements and TCAD simulation with standard model (without incomplete ionization) and with enhanced model (incomplete ionization model)

Introducing the incomplete ionization mechanism delivers results having the same trend as the experiments (Figure 6), clearly demonstrating its impact and importance. Indeed, with this enhanced model, pinning voltage shows a linear decrease between 300K and 150K then a more important drop below 150K. This requires a specific calibration of TCAD tools to be able to analyze the electrostatic conditions in the pixel at low temperature. This pinning voltage reduction potentially impacts both the PPD FWC and the PPD charge transfer conditions.

TCAD analysis with the proper calibration provides a way of looking for potential obstacles along charge transfer path between the pinned photodiode and the transfer gate toward the sense node.

As shown in figure 8 and 9, neither barrier nor pocket does appear at low temperature which could prevent from complete charge transfer. However, despite this fact, caution has to be taken when guessing the dynamic charge transfer behavior based on the assumption of an increased mobility along this path at low temperature. Indeed, the charge velocity at low temperature will by driven by

complex mobility behavior in the sensor implant area featuring a strong dependence on the its doping level [7] and in the transfer gate channel region [8].

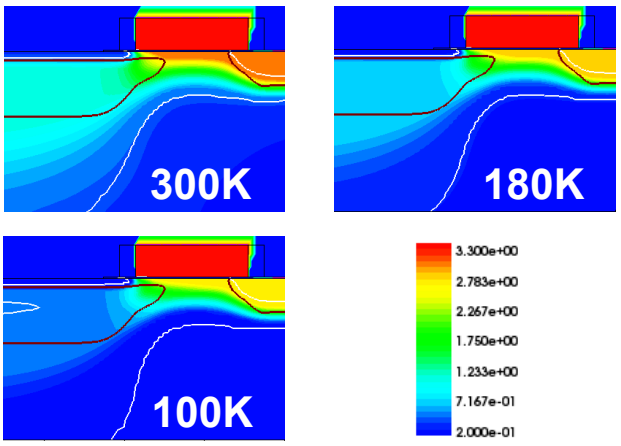

Figure 7: QuasiFermi potential evolution along the PPD and the transfer gate during a transfer with sense node kept at constant voltage for convergence achievements for 3 temperatures: 300K, 180K and 100K.

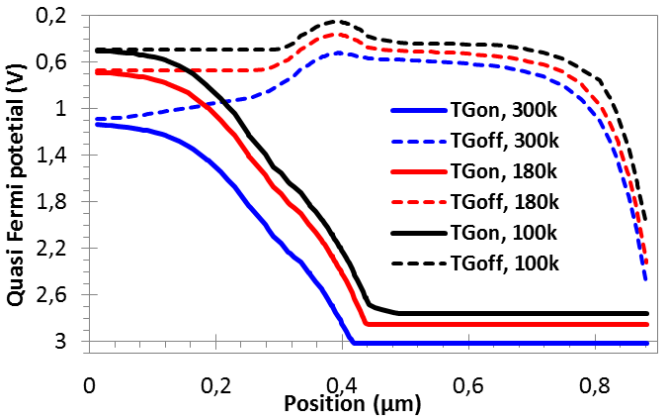

Figure 8: Comparison of the QuasiFermi potential evolution along the PPD and the transfer gate during a transfer "ON" and "OFF" with sense node kept at constant voltage for convergence achievements for 3 temperatures: 300K, 180K and 100K.

III. CRYOGENIC OPERATION IMPACT ON READOUT CHAIN TRANSFER FUNCTION

As depicted in [4], two main parameters impact the features of a MOS transistor used at low and cryogenic temperature:

- Threshold voltage, which increases when temperature is reduced.
- Carrier mobility in transistor's channel, which increases, in this range of temperature and doping level, when temperature decreases leading to a transconductance increase as shown in Figure 9.

In order to understand readout chain behavior and specially the in-pixel source follower transistor, MOS device structures have been designed and measured at low and cryogenic temperatures.

Figure 10 illustrates the threshold voltage measurements for various Source-Bulk voltages (V_{SB}) and for the in-pixel source follower transistor with a W/L=1. As expected, threshold voltage increases when temperature decreases down to cryogenic temperature. We can notice that this

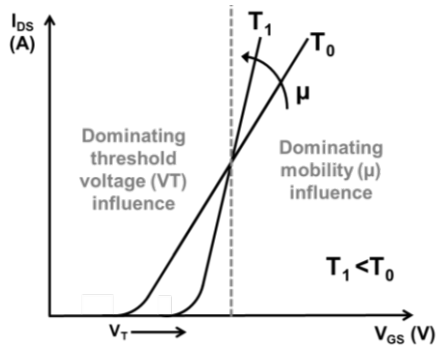

Figure 9: threshold voltage and transconductance theorical evolution in function of the temperature

increase have a relatively weak dependence on the source-Bulk voltage which corresponds to a reduced body effect variation in function of the temperature.

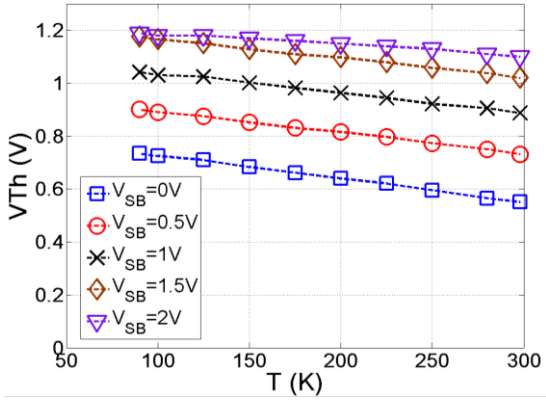

Figure 10: Threshold voltage vs Temperature for different Source-Bulk voltage of the in-pixel Source Follower (W/L=1)

Concerning the transconductance, as also predicted, it is boosted when temperature decreases (Figure 11) with an increase current up to 230% depending of the gate-source voltage.

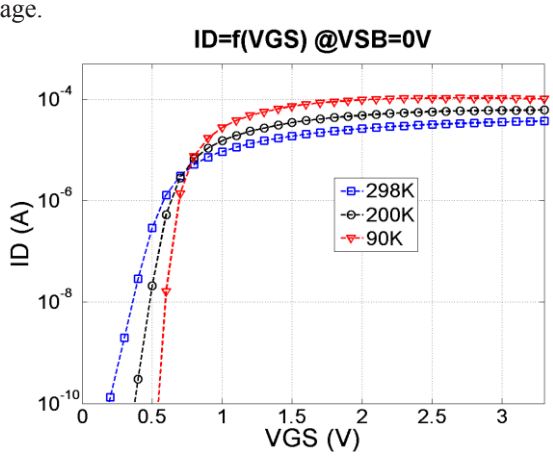

Figure 11: MOST ID vs VGS for 3 temperatures @VDS=100mV (W/L=1)

It has to be taken into account that analog simulations performed with standard foundry models, providing good matching at room temperature, do demonstrate poor representativeness of the cryogenic temperature behavior, as shown in Figure 12 due to the lack of specific low temperature models and associated parameters. There is a clear weakness that will put strong pressure on modeling effort in order to achieve a good confidence on the pixel circuit behavior.

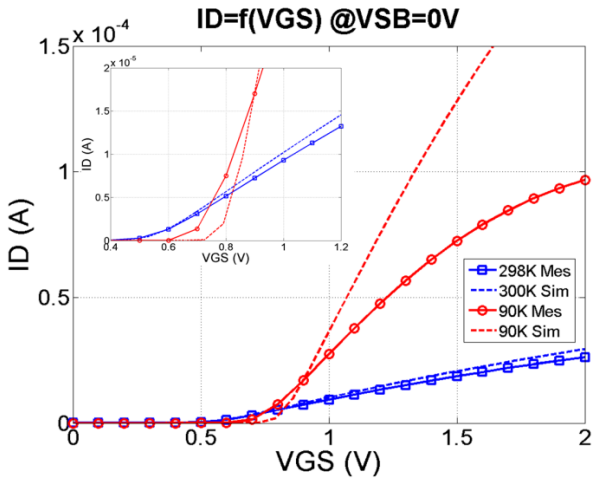

Figure 12: MOST ID vs VGS comparison between measurements and electrical simulations (typical) at 298K and 90K @VDS=100mV (W/L=1)

Table 1 sums up of effects of low and cryogenic temperatures at device and in-pixel readout chain level.

MOSFET	Source Follower	Reset	Row Select
Impact of cryogenic operation at device level	- Increase of VT - Curent variation, (or respectively V_{GS} variation) depending on V_{GS} bias condition (or bias curent condition)	-Increase of VT	-Increase of VT - Curent variation, (or respectively V_{GS} variation) depending on V_{GS} bias condition (or bias curent condition)
Impact of cryogenic operation at readout circuit pixel level	Output voltage swing variation can be increased or decreased (dominating VT or µ influence)→ depends on circuit polarization.	Reduction of reset level value	Variation of R_{DS} (neglected impact on voltage swing and gain)

Table 1 : Impact of low and cryogenic temperatures at device level and at in-pixel readout chain level

Measurements have been performed on our simple image sensor prototype with the complete analog readout chain composed of the in-pixel source follower coupled with the column current source, a sample and hold stage and an output stage (PMOS source follower). Readout chain transfer function measurements (including PMOS output stage) are shown in Figure 13 for three temperatures: 300K, 200K and 80K. As can be seen, the readout circuit works properly with minor changes. The voltage output swing is increased and the gain of the readout chain is only slightly modified at low and cryogenic temperatures.

The lower part of the transfer function, where output voltage swing is enhanced, corresponds to the in-pixel readout circuit (NMOS transistors) limitation. For this stage, the bias current is settled to 5µA at 300K via a constant voltage bias applied to a common column MOS current source. It is important to notice that the observed behavior cannot be generalized. Indeed, due to the threshold voltage and mobility changes opposite influence (Figure 9) when temperature decreases down to cryogenic conditions, different behaviors along temperature can be observed depending on bias conditions (threshold voltage or mobility dominant driving on current-voltage device behavior at low temperature). Without $I_{DS}=f(V_{GS})$ curves of each type of MOS transistors used in the readout chain at cryogenic temperature, it is really uncertain to predict the behavior of the output swing voltage. Conversely, the gain exhibits only a slight variation with temperature (the body effect has been shown on the Figure 10 to be weakly dependent on temperature).

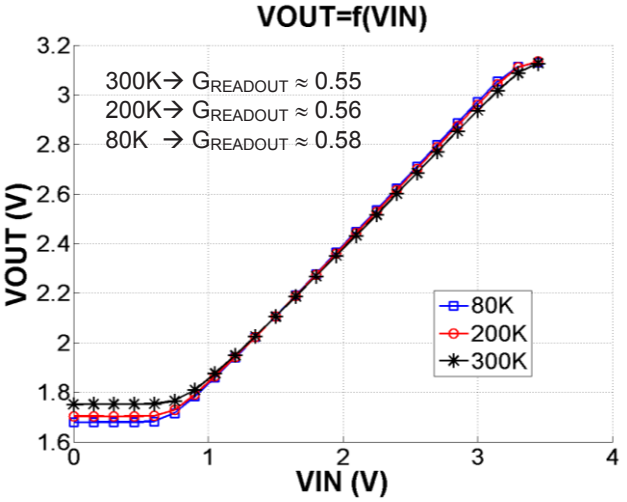

Figure 13: Readout chain transfer function measurements for 3 different temperatures: 300K, 200K and 80K.

IV. CONCLUSION

This work provides a first insight in the PPD pixel behavior at low and cryogenic temperatures. Measurements show a pinning voltage reduction as temperature decreases, in good correlation with TCAD enhanced model simulation taking into account the incomplete ionization phenomenon. TCAD analysis of potential between pinned photodiode and transfer gate shows neither barrier nor pocket which could prevent from complete charge transfer. Further analysis have to be performed to quantify the FWC potential limitations and the charge transfer characteristics (efficiency, speed) evolution especially the impact of mobility variation along the charge transfer path on charge velocity.

REFERENCES

[1] A. Hammoud and al. "Electronic components and circuits for extreme temperature environments" ICECS 2003, pp 44 - 47

[2] S-Y. Wang and al, " The prototype cameras for trans-Neptunian automatic occultation survey ", *Proc. SPIE* 9908, Ground-based and Airborne Instrumentation for Astronomy VI, 990846 (August 2016)

[3] J. Pratlong and al, "A 9 megapixel large-area back-thinned CMOS sensor with high sensitivity and high frame-rate for the TAOS II program ", *Proc. SPIE* 9915, High Energy, Optical, and Infrared Detectors for Astronomy VII, 991514 (August 2016)

[4] Gutierrez-D , Deen , Claeys, "Low Temperature Electronics: Physics, Devices, Circuits, and Applications" , 2001, Acad. Press

[5] A. Pelamatti *et al.*, "Comparison of Pinning Voltage Estimation Methods in Pinned Photodiode CMOS Image Sensors," in *IEEE Journal of the Electron Devices Society*, vol. 4, no. 2, pp. 99-108, March 2016.

[6] A. Pelamatti *et al.*, "Temperature Dependence and Dynamic Behavior of Full Well Capacity in Pinned Photodiode CMOS Image Sensors," in *IEEE Transactions on Electron Devices*, vol. 62, no. 4, pp. 1200-1207, April 2015.

[7] S. Li, W.Thurber, "The dopant density and temperature dependence of electron mobility and resistivity in n-type silicon', Solid.State Electronics, 1977, Vol. 20, pp. 609-616.

[8] J.S. Duster, Z.H. LiA P.K Ko, and C. Hu, "Temperature Effects of the Inversion Layer Electron and Hole Mobility of MOSFETs from 85K to 500K", 1993 International Conference on Solid State Devices and Materials, pp. 835-83