Toward one Giga frames per second: Multi-Collection-Gate BSI Image Sensors

by Takeharu G. Etoh[1], Son V. T. Dao[1] , Tetsuo Yamada[2] and Edoardo Charbon[3]

[1]Ritsumeikan University, Noji-Higashi 1-1-1, Kusatsu, 525-8577 Japan

Tel: +81(0)77-561-5052; E-Mail: etoh@fc.ritsumei.ac.jp

[2]Tokyo Polytechnic University, Atsugi, Japan

[3]Technische Universiteit Delft, Delft, the Netherlands

Abstract The ISIS is the ultra-fast image sensor with pixel-based storage. To achieve higher sensitivity, a BSI ISIS was developed. To avoid direct intrusion of light and migration of signal electrons to the storage area on the frontside, a cross-sectional sensor structure with thick pnpn layers was developed, and named "Tetratified structure". To achieve much higher frame rate, a multi-collection-gate (MCG) BSI image sensor architecture is proposed. The photoreceptive area forms a honeycomb-like shape. Performance of a hexagonal CCD-type MCG BSI sensor is examined by simulations. The highest frame rate is theoretically more than 1Gfps. For the near future, a stacked hybrid CCD/CMOS MCG image sensor seems most promising. TSV process is the key technology to realize the structure.

1. BSI ISIS

The in-situ storage image sensor, ISIS, with a slanted linear in-situ storage CCD achieved 1Mfps in 2001[1)]. However, the storage area in each pixel covered with a light shield reduced the fill factor to 15%. To improve the fill factor to 100%, a BSI ISIS structure was developed[2)]. The cross-sectional architecture is depicted in **Figure 1**. **Figure 2** shows an example potential profile. The frame rate was also significantly increased to 16Mfps for 165kpixels by metal wiring on the frontside with more freedom in the design[2)].

To prevent direct intrusion of incident light into the storage area on the front side, the thickness of the sensor was increased to more than 30um. For the thickness of 30um, 0.1% of the 700nm incident light still reaches the front side. Technology to produce a thicker and low-concentration epi-layer with fewer defects is awaited.

To avoid migration of the generated electrons to the storage area of each pixel, a p-well embracing the n^+ CCD storage channels is formed in the n^- epi-layer grown on a p^- epi-layer. The structure with n^-/p^- double epi-layers reduces the backside bias voltage to deplete the photoelectron path to the frontside, which yields less electric field and thus suppresses dark current during the image capturing operation. The structure consisting of the $p^-/n^-/p/n^+$ layers was named a "Tetratified" BSI image sensor structure, where "Tetratified" stands for "tetra-stratified". In the p-well, various functional circuits other than the in-situ storage can be installed.

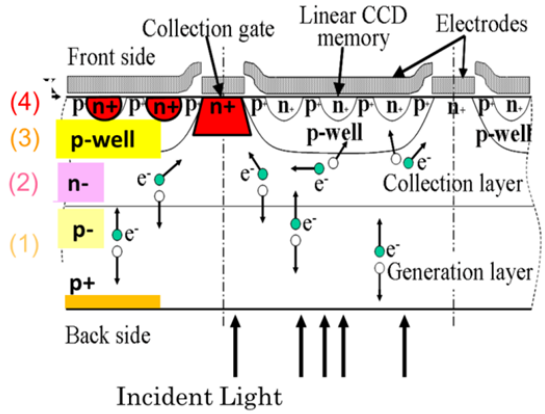

Figure 1 A BSI ISIS with a "Tetratified" structure

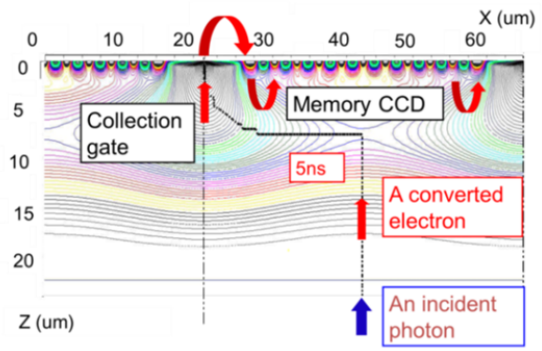

Figure 2 A potential profile and an electron path

2. Multi-collection-gate Image Sensor

2.1 Macro-pixel Operation of Quad-collection-gate Image Sensor

The frame rate can be quadrupled by grouping pixels of an ISIS type sensor to macro-pixels, each with independently operated 2x2 subpixels, and by operating them in turn. Usually, the travelling time of a photoelectron to a collection site of a subpixel is shorter than the transfer time of the collected image signal charge to the in-situ storage. If the transfer time is less than three times the travelling time, an image signal collected at one of four subpixels is transferred completely to the storage area during collection of image signals at the other three subpixels.

The disadvantage is that, during the collection of photoelectrons in one of the subpixels, photons incident to the other three are drained, and therefore, the fill factor of the macro pixel becomes less than 25%.

The tetratified BSI structure solves the problem. A conceptual model of the pixel is shown in **Figure 3**. Four collection gates of the subpixels are centered, to each of which an in-situ storage CCD is attached. They are protected from the migration of signal electrons by a p-well built with a couple of the masks shown in **Figure 4** (rotated). The p-well has an n-type hole at the center, and is thicker at the periphery of each pixel and thinner toward the center, which creates a potential gradient to the center and nicely accelerates electrons toward the center. The 3D potential profile created by the p-well and the epitaxial layers works as *an electronic microlens*. The fill factor is now 100%. Electrons passing through the central hole are collected by one of the four collection gates where a higher voltage is applied, which enables selective signal collection by one of the multi-collection gates.

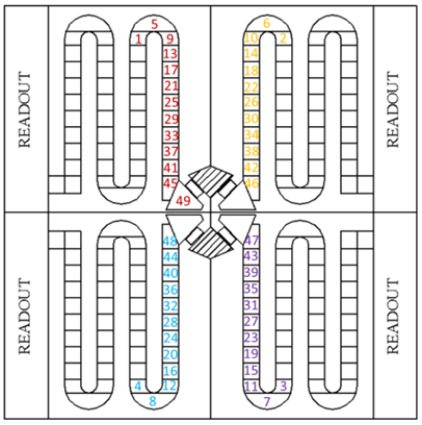

Figure 3 Tetragonal MCG BSI CCD image sensor

2.2 Honeycomb Multi-collection-gate Image Sensor

When the number of collection gates in a pixel is six or eight, the shape of the pixel becomes hexagonal or octagonal as shown in **Figure 5** and **10**. When the imaging area is filled with pixels, the photo-receptive area forms a honeycomb-like shape.

Figure 5 shows a pure CCD sensor with hexagonal pixels. To make the pixel grid square, the hexagons are distorted. **Figure 10** shows a model of the frontside circuit of a stacked hybrid CCD/CMOS image sensor with octagonal pixels. The image sensors with the structure are named ‘Multi-Collection-Gate Backside-Illuminated image sensors (MCG BSI image sensors)’.

3. Preliminary Simulations

The core technology of the MCG BSI image sensor is selective collection of signal electrons by one specified collection gate, which is also the most difficult part in the design. To prove the validity of the technology, preliminary simulations were conducted for a hexagonal MCG BSI image sensor. By covering the frontside circuit with a deep p-well made with a couple of masks shown in **Figure 4**, signal electrons generated by incident photons to the square area shown in **Figure 6** are collected by one of the collection gates. A collection gate consists of an entrance gate and a storage gate, followed by an exit barrier gate and a transfer gate. All the gate structure is the buried CCD.

Direction of the second metal wires is parallel to that of the pixel boundary as shown in **Figure 6.** The size of a pixel is 10.8um. Eighteen metal wires are necessary to deliver voltages to drive a pixel. For 0.13um process, the pitch of the second metal wires was fixed at 0.6um with some allowance, which determines the size of the pixel (0.6um x 18 = 10.8um). The thickness of the chip is 33 um, which consists of an 11um n-epi and a 22um p-epi layers.

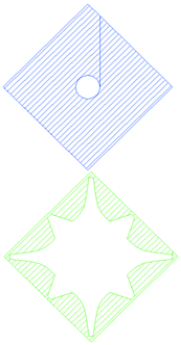

Figure 4 p-well masks

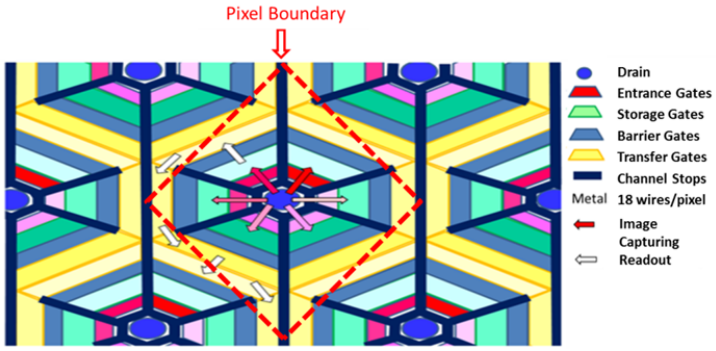

Figure 5 Hexagonal MCG BSI CCD image sensor

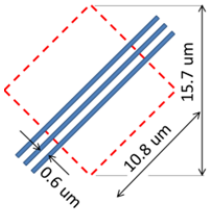

Figure 6 Pixel dimension

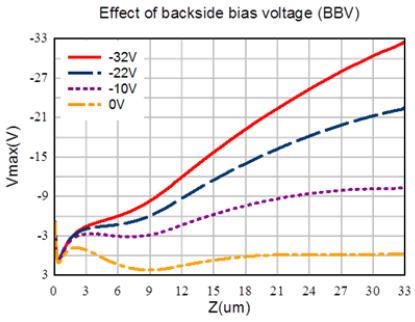

Figure 7 Z-direction potential profiles at the center vs. backside bias voltages

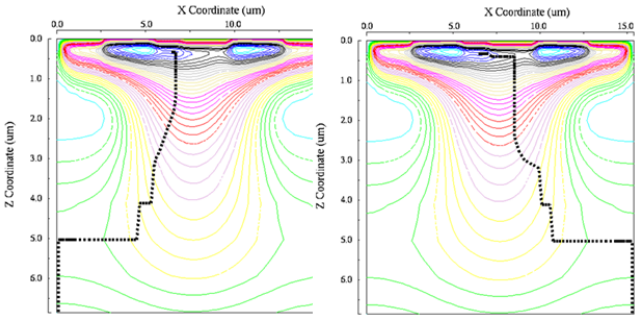

Figure 8 Paths of an electron from the left and right corners of the pixel to the left collection gate

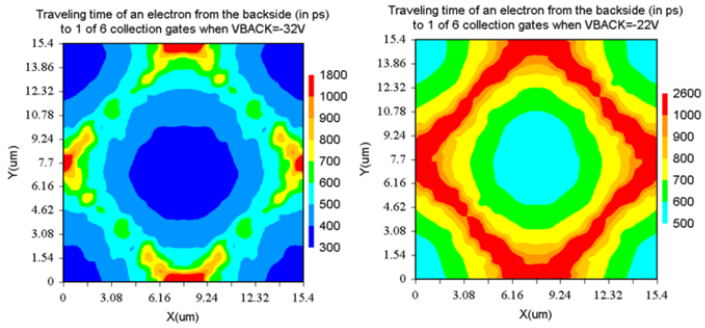

Figure 9 Travel time distribution (ns) of an electron from the backside to a collection gate
Backside voltage: left; -32V, right; -22V

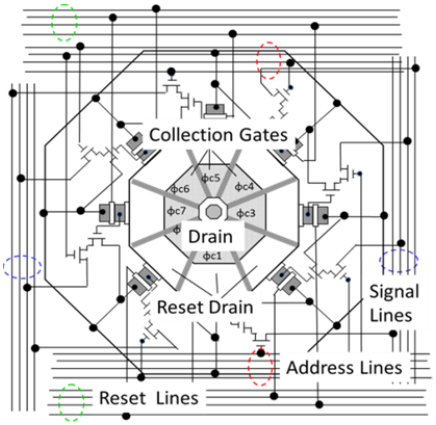

Figure 10 Octagonal stacked CMOS MCG BSI image sensor

During the image capturing operation, voltages of all storage gates are kept at the high level. When the voltage of one of the entrance gates is raised, keeping the others at the low level, the signal electrons are collected by the collection gate through the raised entrance gate.

Figure 7 shows potentials in the depth (z) direction at the center of a pixel. If the backside voltage is lower than -22V, the signal electrons safely travel to the frontside; if it is higher than -10V, the signal electrons can no longer directly go to a collection gate, being blocked by a potential dip in the path.

Figures 8 shows paths of an electron generated at the left and the right corners of a pixel. The voltage of the left-side entrance gate is at the high level. **Figures 9** shows the travel time distribution of an electron from a point of the backside to a collection gate. It depends on the backside voltage as well as the generation site.

For the backside voltage -32V, more than 95% of signal electrons reach the collection gate in less than 1ns, and, thus, practically, 1Gfps is achievable. However, an electron generated at the left or right corner of the pixel shown in **Figures 6** takes more than 1.5 ns. The time can be reduced to less than 500ps by collecting the incident light to the central area of a pixel with an optical microlens. For the backside voltage -22V, the microlens is necessary to achieve 1Gfps. However, the dark current reduces for the less electric field from the backside to the frontside as shown in **Figure 6**.

4. Concluding Remarks

The performance indices targeted by the MCG BSI image sensors are shown in **Figure 11** with those of high-speed image sensors previously reported.

Toward 1Gfps, many problems lie to be solved; effective in-pixel signal amplification in a very short time, synchronized exact timing control, in-situ digitization, and so forth. Allocation of these functions to chips of a stacked-chip image sensor seems promising for effective integration of the functions. A fine TSV process is the key technology to realize the dream.

This work is supported by JST A-STEP [FS] stage; Exploratory Research.

References

[1] Etoh et al., A CCD image sensor 0f 1Mfps for continuous image capturing of more than 100 consecutive frames, *Digest of Technical Papers, ISSCC2002*, 45, pp.46-47, 2002.

[2] Etoh et al., A 16 Mfps 165kpixels backside illuminated CCD, *Digest of Technical Papers, ISSCC2011*, 54, pp.406-407, 2011.

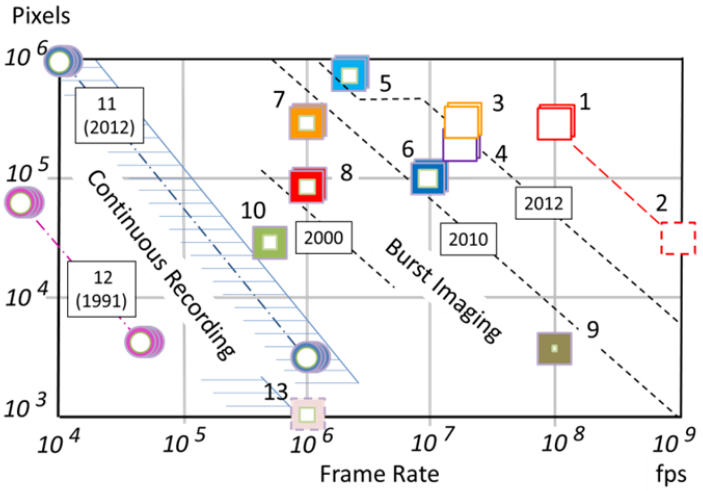

Figure 11 Evolution of high-speed image sensors: frame rate, pixel counts, fill factor, number of frames and years of developments

White square: fill factor

Number of frames: 2-9, 10-99, 100-999 and 1,000-

1 and 2: Targets of the MCG BSI image sensor proposed in this paper: 1. Tetragonal (Figure 3), 2. Hexagonal (Figure 5) 3: Arai, et al., SPIE8659-3, Linear CCD, BSI 4: Etoh, et al., ISSCC2011, 54, 406-407, Linear CCD, BSI, with EM-CCD 5: Crooks, et al., SPIE8659-2, SPS CCD/CMOS Readout, FSI 6: Tochigi, et al., ISSCC2012, 55, 382-383, CMOS, FSI, Periphery storage 7: Ohtake, et al., Broadcast Tech., 28, 2-9, Linear CCD, FSI, Color 8: Etoh, et al., ISSCC2002, 45, 46-47, Linear CCD, FSI 9: Lazuvsky et al., SPIE5787, 184 10: Kosonocky, et al., ISSCC1996, 39, 182-183, SPS CCD, FSI 11: CMOS, FSI, most advanced continuous recording high-speed cameras; by partial readout, the frame rate distributes in a wide range; several models. 12: Etoh, Continuous recording, the first commercially available digital-recording high-speed video camera, NMOS, FSI 13: El-Desouski, et al., Sensors, 9(1), CMOS, FSI, 8 frames (The mark represents the experimental result. The paper claims possibility of 1.25Gfps) (14. Kleinfelder, et al., IEEE Trans. Nuclear Sciences, 56(3), CMOS, 4Mfps for 32 frames with CDS; 12x12 pixels (the mark is below the range of the figure)