Cmos Image Sensor Pixel with 2D CCD Memory Bank for Ultra High Speed Imaging with Large Pixel Count

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Abstract - We present the design and optimization of a 30um CMOS Image Sensor (CIS) pixel. This pixel is embedded in a sensor working in burst mode at speeds up to 5Mfps and high resolution (0.7Meg). Such performance is achieved using two dimensional CCD Memory bank at each pixel which was manufactured using a 0.18um well established CIS Process.

***Keywords*— CCD in CMOS, Buried Channel, Charge Transfer, Global Shutter, CDS.**

I. INTRODUCTION

In recent years a few examples of ultra high speed sensors have emerged. Most of them use the concept of very short exposures and fast sequential storage in a Memory Bank (MB); a MB is placed in each pixel element. This concept and the demonstration of the first imager was published in 1996 by Kosonocky et al 0. More recently the concept was reused in the ISIS[2-4] sensor family, achieving 16 million fps on a 362x456 pixel sensor with 117 memory cells per pixel. Basically, these devices are manufactured using a CCD which limits the readout time and repetition rates. Moreover, there is no continuous operation mode which excludes some applications. Other sensors are fabricated using MOS capacitor bank in CMOS technology [5-6], but these devices have limited performance as well as a small MB depth. The new approach, described in this paper utilizes the benefits of advanced node CMOS fabrication technology for CCD device manufacturing [7,8]: (a) Narrow poly to poly gap; (b) Efficient fill of the poly to poly gap by nitride spacers. These eliminate the need for using overlapping poly structures traditionally used in CCD fabrication, and allowed us an efficient design of the multiple storage pixels - implemented as a compact CCD manufactured in 0.18um CMOS node [8]. In this paper we present the pixel design. We show experimental results which demonstrate full transfer of electrons from the pinned diode through the 2D CCD array to the readout, at speed which supports frame rate up to 5Mhz. The design of a sensor which is based on the pixel presented here and its performance are discussed in [9].

II. PIXEL STRUCTURE

The pixel's block diagram is shown in Figure 1. It consists of five building blocks: i) a fully pinned photodiode (PD) which was optimized for fast transfers below 100 nsec; ii) the PD to CDD Memory Bank (MB) input structure; iii) the two dimensional MB; iv) the output structure of the MB to the floating diffusion (FD) and v) the pixel readout circuit. The in-pixel CCD MB is created using a 180 nm CMOS Image Sensor process with dual oxide of 3 nm and 10 nm from TowerJazz [10]. The imaging array and in particular the MB electrodes are using the 10 nm gate oxide which allows applied voltages up to 6V. The MB has a total of 180 memory cells organized as follows:

- A vertical entry (VEN) bank with 10 cells
- Ten rows of lateral (LAT) banks, each with 16 cells
- A vertical exit (VEX) bank with 10 cells

The MB is based on three phase CCD operation. This was considered a good compromise between number of pixel control lines and memory cells density per unit area. Each cell unit in the MB has three separate polysilicon electrodes. The integrated charges are coupled from the diode into the MB through a single electrode (PGEN).

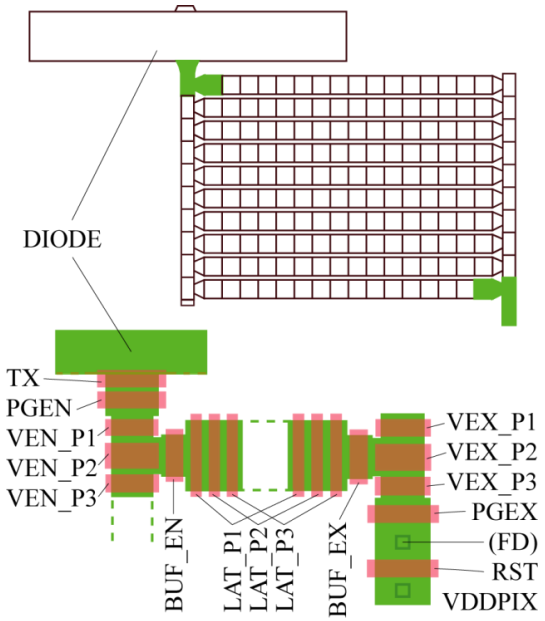

Figure 1 Pixel Block diagram

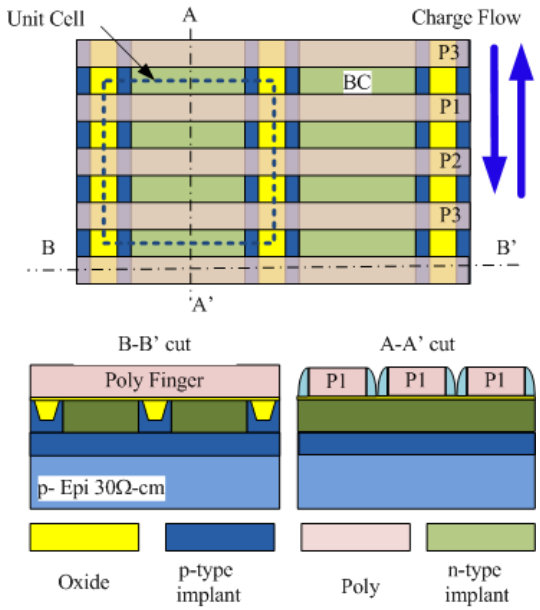

Figure 2 Illustration of MB CCD cell

The charges are first distributed vertically in the MB by a VEN bank. Each time VEN is filled, the charges are pushed laterally to the LAT bank through a tapered single electrode (BUF_EN). The tapering is designed to overcome the different dimensions of the VEN and LAT registers. Moreover when BUF_EN is deactivated the VEN and LAT are decoupled which allows charge location manipulation both in the vertical and lateral direction. Similarly a single tapered electrode (BUF_EX) couples between the LAT and VEX banks. The VEX is used to move charges towards the FD, which is coupled to the VEX by a single gate electrode (PGEX). Defining the number of cells in the vertical (lateral) banks as nV (nL), the depth n_{MEM} of MB is simply given by:

$$n_{MEM} = n_V * (n_L + 2)$$

The separation between poly electrodes is 250 nm, each poly edge is associated with nitride spacer so effectively the poly to poly gap is filled with Si_3N_4, which is a key in enhancing the fringing fields. The poly silicon electrons are non- salicided. A special pre-etch poly doping step is performed before the poly etch to avoid implant between the poly fingers which could later be a problem during charge transfer. Illustration of the CCD MB cell is presented in Figure 2. The channels are separated with the foundry standard Shallow Trench Isolation (STI). The buried channel n-type implant is isolated from the STI by a dedicated p type implant. The buried channel and the p-type barrier implant where carefully simulated in TCAD and MEDICI.

Simulation of a 1D potential cut in the middle of the one of the phases cell are shown in Figure 3. The implants were optimized to give: i) fully depleted channel potential of about 1V; ii) location of potential maximum ~ 0.1µm below the gate oxide (GOX) and iii) a capacity of about 10 ke- for a 0.4 µm2 gate at 1V. Figure 3 also shows that for 5V on the gate. The device becomes a surface channel one. Simulations were also used to optimize the design of the one directional transfer of electrons from the diode to the MB as well as to the design of the PGEN and PGEX gates. TowerJazz uses common surface Transfer Gate (TX) and lots of simulation and experimental effort invested in optimizing the transfer between the pinned diode through the surface device and into the buried channel.

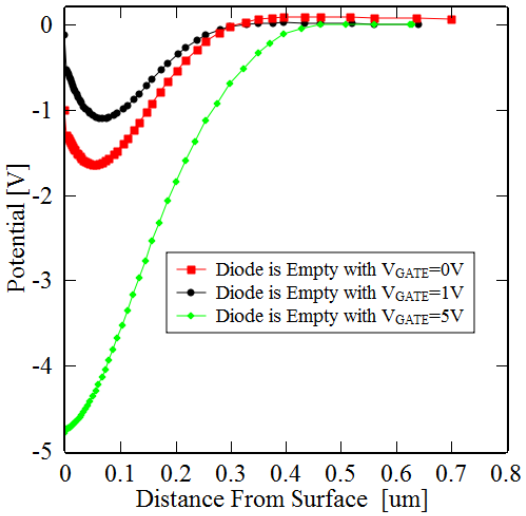

Figure 3 One Dimensional Potential pofile of the buried channel, taken from the middle of the poly finger

In order to achieve frame rate in excess of 2 MHz, the exposure time for this imager has to be smaller than 500 nsec. This dictates very short transfer time from the pinned diode to the MB. The pinned diode is carefully optimized to ensure full charge transfer in less than 100 nsec. The diode space is very limited and elongated in order to maximize the fill factor with the scalable MB architecture. Because of these constraints and the pixel size of 30 µm, the diode had to fit in to an area of about 28 µm in the horizontal direction and 5 µm in the vertical direction. The electrons are collected from the whole area and transported to the vicinity of TG thanks to a graded potential profile. The profile is achieved with only one diode n- implant which is optimized to have strong side wall depletion. Top view schematic of graded pinned diode is shown in Figure 4. It can be seen that the n- implant is drawn with different W along the diode, the smallest W is drawn on the diode far side while the maximum width is drawn between the TG and AB gate. The highest potential is designed to be about ~1.2 V, and the smallest potential is about ~0.3 V. This potential gradient drives the collected photo-electrons to the vicinity of the TG during the exposure period which reduces the transfer period due to the strong interaction of the electrons with the electric field induced by the TG. The diode is surrounded by a guard ring which is connected to a high potential: this prevents diffused electrons which are not collected from the PD to be collected in the MB.

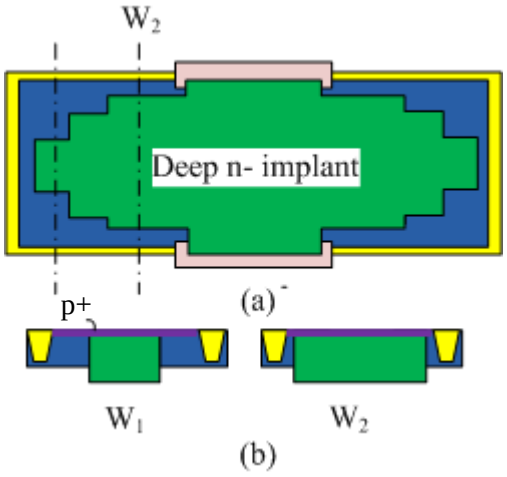

Figure 4 Illustration of the graded profile fully pinned PD

III. EXPERIMENTAL RESULTS

A schematic of tapered voltage timing which was used to ensure full transfer at 200nsec time scale is shown in Figure 5. The transfer starts with all charges localized under the Departure Gate (DG) with voltage of 3.5V, the Arrival Gate (AG) is at 0V. At time T1 we ramp the voltage on the AG to 3.5V, so the charge packet is now spread between the two electrodes. At time T3 we ramp up the AG to 4.5V and ramp down the (DG) to 0V, most of the electrons are now placed under the AG. To ensure full transfer, at time T4, DG is ramped down to -1V while keeping the AG at 4.5V. At T5 we complete the cycle. The DG is ramped to 0V and the charge packet is now localized under the AG with 3.5V. The total time for full transfer from (DG) to (AG) is less than 500nsec. The optimization of the Tapering sequence timing segments is shown in Figure 6.

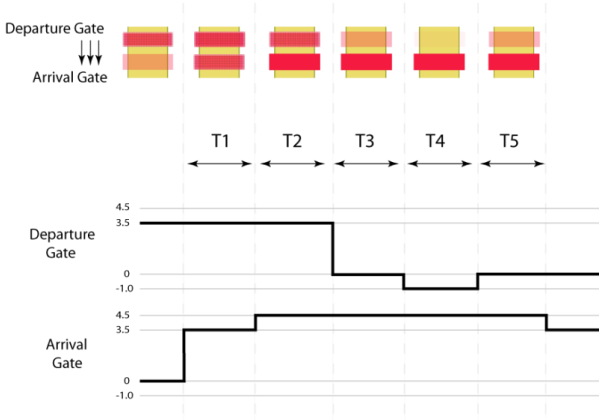

Figure 5 Illustration of the tapered voltage timing scheme

The transfer of electron from diode through the Surface Channel is handled in a similar way but maximum voltage on the Transfer Gate should not exceed 3V. Over driving the TX leads to strong localization of charges under it and severe image lag problems. The transfer of electrons into the FD is handled by strong over drive of the RESET transistor and setting the (FD) to the highest voltage which is still handled by the readout circuits; it was found that ~5V gives on the FD will give sufficient results.

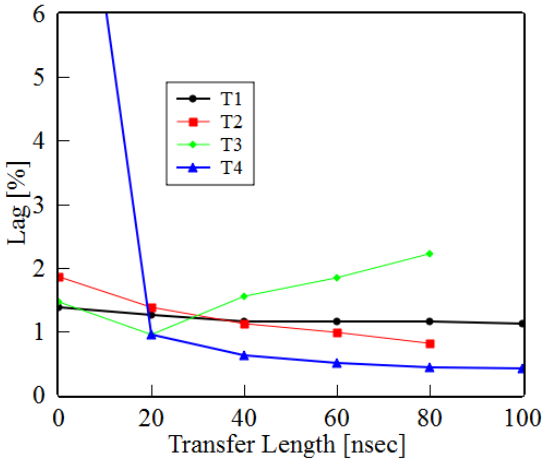

Figure 6 Optimization of Transfer Sequence timing

Finally, we look on AB and TX pulse length which also sets the limit to the max achievable Frame Rates. In Figure 7 it is shown that for TG pulses >70nsec the output signal saturates. In Figure 8 it is shown that overall LAG (Diode and CCD chain) measured from 50% bright to dark is under 1% for AB pulse length >150nsec.

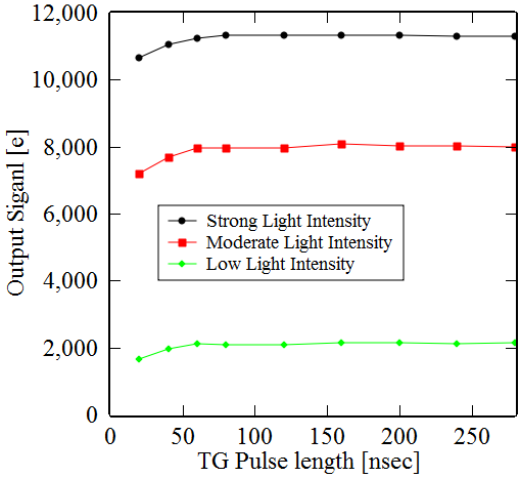

Figure 7 Output signal as a function of pulse length.

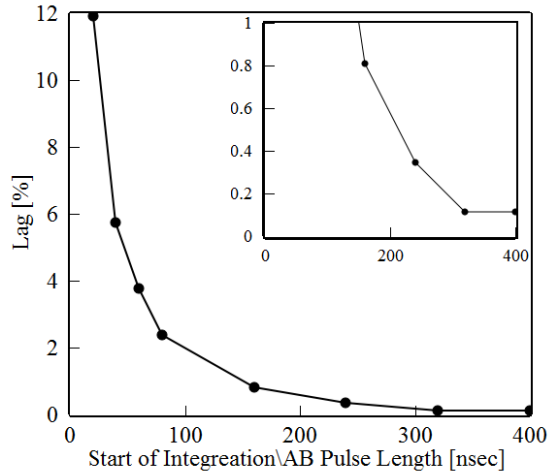

Figure 8 Lag as a function of AB pulse length (half full well in the previous frame)

IV. CONCLUSIONS

In this paper we have presented the design and timing optimization of a 30um CMOS Image Sensor pixel intended for ultra-high speed imaging. The pixel is using a dedicated 2D CDD memory Bbnk and high speed pinned photodiode both are shown to successfully operate in time scales appropriate for 5Mfps imaging. The pixel is used in a prototype sensor which is currently under evaluation in a dedicated high speed camera system by Specialised Imaging [11].

V. REFERENCES

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