CMOS Image Sensor for 3-D Range Map Acquisition With Pixel-Parallel Correlation In Region of Interest

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Abstract—An image sensor for 3-D range map acquisition with pixel-parallel correlation in the region of interest is presented. By the use of modulated sheet light projection and correlation technique, the sensor can suppress background illumination. In order to achieve high resolution, correlation circuits is put outside of 128×128 pixel array, one in each column and 16 in each row. The sensor finds the columns which includes activated pixels by column-parallel correlation circuit and next searches the illuminated position within the region by the row-parallel correlation circuit block. The correlation circuit achieves -18 dB signal-to-background ratio (SBR) and 76 dB dynamic range in simulation. The frame rate is estimated to be 200 - 500 fps.

I. INTRODUCTION

At present, 3-D images are used in various applications, including a vision sensor of robots, medical applications and amusement by gesture recognition, and the techniques to get more accurate 3-D information at high speed is required. There are several techniques to acquire 3-D data. The stereo-matching method can obtain 3-D information from only 2-D information. However, it takes long time to calculate instead of using special equipments. The techniques using light source can solve this problem. The time-of-flight(TOF) method calculates range by lap time of light between the target object and the sensor[1][2], but it is difficult for this method to obtain 3-D information at close range. Then, the light-section method using sheet light can obtain high accurate 3-D range maps by simple calculation based on triangulation[3][4][5]. It, however, needs strong laser light in order to distinguish it from background illumination. Therefore, it is difficult to use this method with safe illumination level for human eyes. One solution of this problem is correlation techniques. This technique uses modulated sheet light and can suppress background illumination by detection in frequency domain. However, a pixel circuit of this scheme becomes large due to complex detection circuits and resolution is degraded. In this paper, we propose a 128×128 CMOS image sensor with row-parallel correlation circuit block to realize correlated sampling of 16 column ROI block simultaneously.
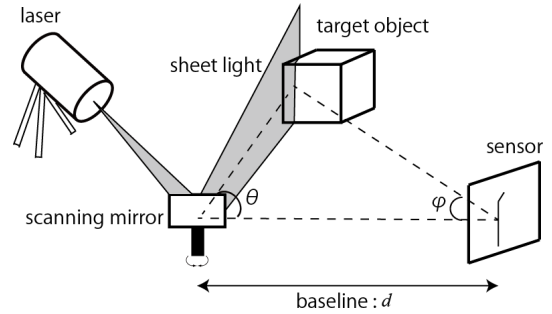

Fig. 1. The Light-Section Method Based on Triangulation

II. PRINCIPLE OF SENSING SYSTEM AND CHIP DESIGN

A. Sensing System Using Light-Section Method

Fig.1 shows a configuration of the light-section method based on triangulation. The sensing scheme uses a laser source, a scanning mirror and an image sensor. The sheet light projected by a laser source sweeps the target surface by a scanning mirror, and an image sensor obtains the position of the sheet light in each scan. The range data is calculated by the light projecting angle, the light incidence angle to the sensor and the baseline length between the sensor and a scan mirror based on triangulation. Therefore, only the decision whether the incident light includes projected light or not is needed in each pixel. The correlation technique is one method to obtain the position of activated pixels against strong background illumination[4][5]. However, it requires complex circuit and thus pixel becomes large, which means low resolution. Our presented ROI search realizes more accurate sensing using the correlation technique.

B. Correlation Circuit and Simulated Result

The sensing system consists of pixel circuits and correlation circuits. Fig.2 shows a schematic of the pixel and correlation circuit, which has a log-response circuit, an adaptive

modulation amplifier, a sampling circuit and a comparator[5]. Photo current gives output voltage V_{pd} in logarithmic response to its value. The log-response circuit extends dynamic range measurement. The average level V_{avg} is generated by a low pass filter and subtracted from the pixel output V_{pd}. Therefore, AC component of V_{pd} is amplified to V_{mod}, and V_{mod} is amplified again to V_{amp} by a differential amplifier. V_{amp} is sampled to two capacitors by two signals $MPY+$, $MPY-$ which synchronize with modulated frequency, shown in Fig.3. As Fig.3 indicates, when modulated light is projected on the pixel plane, the difference voltage between $V+$ and $V-$ is acquired. Alternatively, when the incident light contains only background illumination, the difference voltage is zero. Then $V+$ and $V-$ are compared by a comparator and activated pixels are detected.

The sensitivity and dynamic range of the correlation circuit is simulated. The sensitivity of the correlation circuit is evaluated as signal-to-background ratio (SBR). The photo current is in proportion to light intensity, so we define $20 \log I_{sig}/I_{bg}$ as SBR. I_{sig} is photo current by projected light, and I_{bg} is photo current by background illumination. Fig.4 shows SBR and dynamic range of the sensor estimated by simulation when modulation frequency is 2 kHz. The minimum SBR is -18 dB and dynamic range is 76 dB. The minimum detectable intensity of projected light is defined as I_{sig} when amplitude of pixel output V_{pd} is 10 mV, taking account of noise.
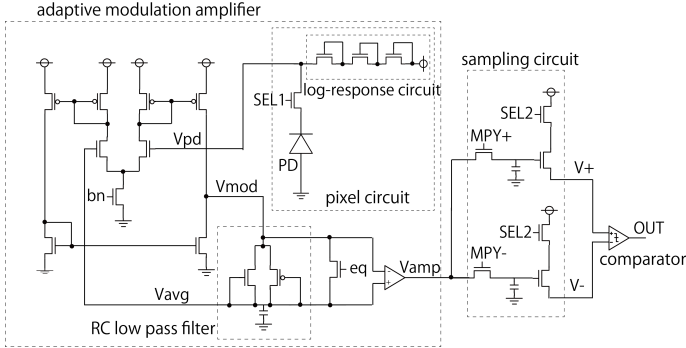

Fig. 3.   Timing Diagram

Fig. 2.   Pixel Circuit and Correlation Circuit.

Fig. 4.   SBR and Dynamic Range.

C. ROI and Row Correlation Readout Block

Fig.5(a) shows the system configurations. A pixel has two outputs, in the column and row direction respectively. In each column, 128 pixels are connected to one correlation circuit, shown in Fig.5(b). Each row is divided into the regions, N pixels in each. N pixels in each region are connected to N correlation circuits on the residue system, shown in Fig.5(c). Our sensor reads out pixels in ROI by N columns block to row-parallel correlation circuits.

D. ROI Block Size and Performance Optimization

In this system, demodulation time in correlation circuit is dominant time for 3-D range map acquisition, thus speed of
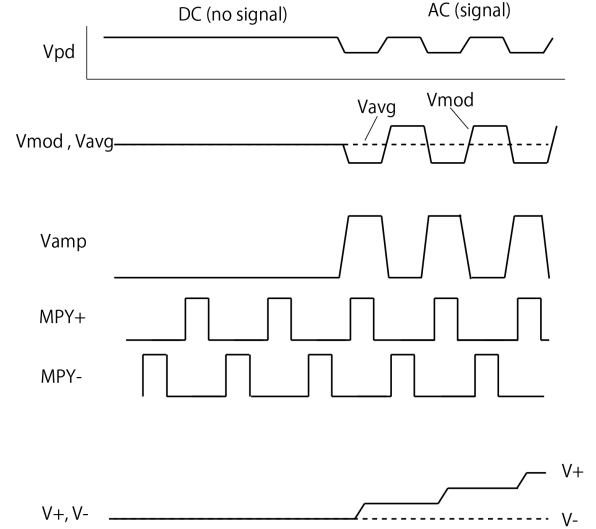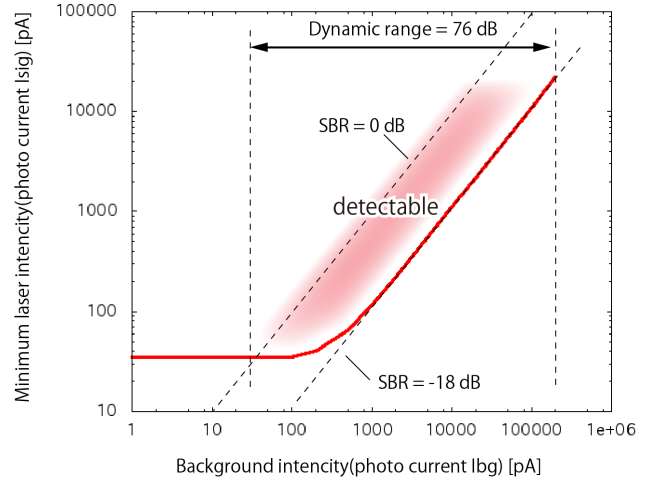
3-D position detection depends on the number of blocks which reflected light traces. We can estimate it by analyzing the field of vision of the sensor and the size of the target object, and optimize N columns block size. Fig.6 shows a bird's eye view of the light-section method. The x axis is width and z axis is depth. When sheet light is projected between the depth z_0 and z_1 on the target plane, the width of activated pixels w is calculated as follows.

$$w = df \cdot (\frac{1}{z_0} - \frac{1}{z_1})$$

The parameter f is focus distance of a lens and d is baseline distance. We calculated the number of activated pixels in the width direction N_w according to $z_1 - z_0$(target size) when f is 8 mm, d is 200 mm and z_0(target distance) is 1000 mm, as shown in Table I. The field of vision is 146 mm.

Based on Table I, we define 16 columns as the ROI block. Therefore, 128×128 pixel array has 8 ROI blocks. The
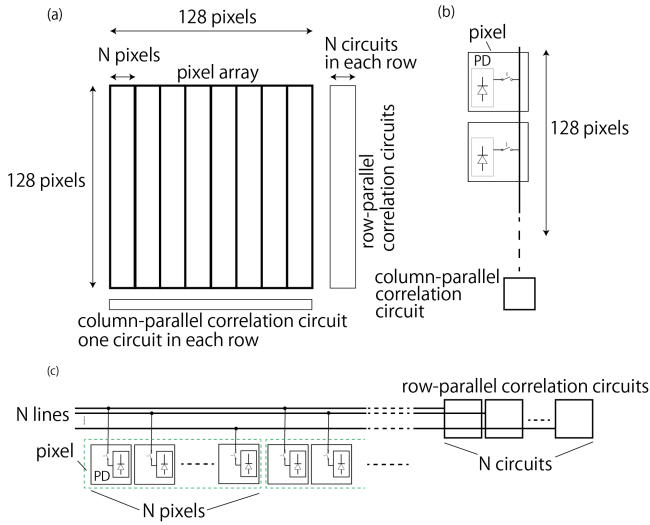
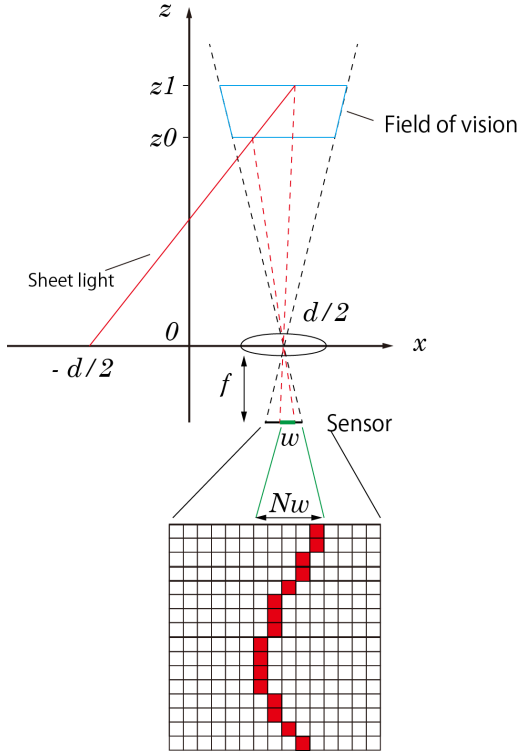Fig. 5. System Configuration. (a) Global image. (b) Column Connection. (c) Row Connection.

Fig. 6. Field of Vision.

system obtains 3-D range map as follows:

1) Connect all pixels to the column outputs at same time in each column. Outputs of column correlation circuits give the columns which includes activated pixels, i.e. ROI, shown in Fig.7(a).

2) Connect the blocks which contains ROI to row correlation circuits in order from left, shown in Fig.7(b). When reflected light spreads over less than 16 columns but two regions, connect those two regions at the same time,

$z_1 - z_0 [mm]$	40	80	120	160
N_w	7	13	19	25
frame rate [fps]	500	500	200-333	200-333
range maps/s [rps]	3.9	3.9	1.6-2.6	1.6-2.6

shown in Fig.7(c). In conjunction with column outputs, the position of reflected light on the sensor plane is detected.

If the target is the largest sphere within the field of vision, the sensor obtains 3-D range map at 3.9 rps.

III. CHIP DESIGN AND EVALUATION

The sensor has been designed and fabricated in 0.18μm CMOS process. The pixel area is 9.14μm $\times$ 9.14μm with 23.5% fill factor. The die size is 2.5 mm $\times$ 2.5 mm. Fig.8 shows the layout of our chip.

The specification of the sensor which is estimated by simulations is summarized in Table II.

TABLE II
SPECIFICATION OF THE SENSOR

Process	0.18 μm CMOS
Chip size	2.5 mm $\times$ 2.5 mm
Resolution	128 $\times$ 128
Pixel size	9.14 μm $\times$ 9.14 μm
Fill factor	23.5%
Sensitivity(SBR)	-18 dB SBR
Dynamic range	76 dB
Light detection rate	200-500 fps
Depth resolution	5.7 mm at 1000 mm

IV. CONCLUSION

A 128 $\times$ 128 image sensor with pixel-parallel correlation in region of interest has been presented. It detects activated pixels in two steps. First, it detects the columns which includes activated pixels by column-parallel correlation circuit. Second, it searches the illuminated position within the region by the row-parallel correlation circuit block. We realize - 18 dB SBR and 76 dB dynamic range in simulation. The speed is estimated to be 200-500 frames per second.

(a)

pixel array

reflected light

column-parallel
correlation
circuit

binary outputs 0 0 0 0 0 0 1 1 1 1 0 0 0 0

Outputs give the ROI

(b)

ROI row-parallel
correlation
circuit ROI block

connect connect

(c)

right block result

left block result

ROI

We can distinguish left block result
and right block result by column-parallel
detection (a)
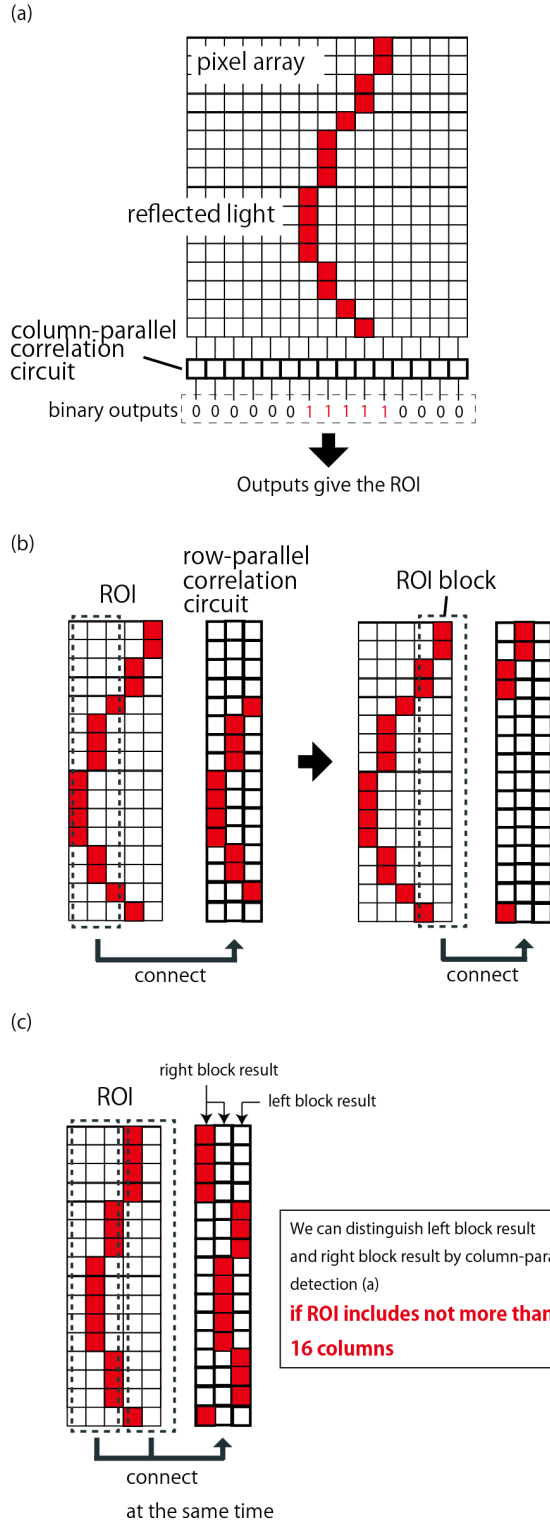
**if ROI includes not more than
16 columns**

connect

at the same time

Fig. 7. System Operation. (a) Column Detection. (b) Detection in Region
of Interest. (c) Two Regions Connected at Same Time.

row-parallel
correlation circuit

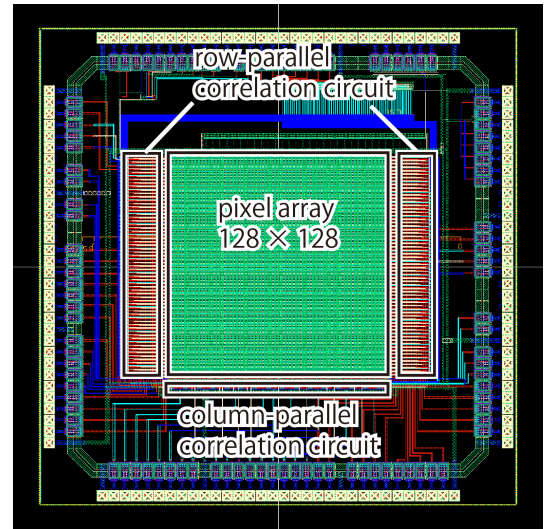pixel array
128 × 128

column-parallel
correlation circuit

Fig. 8. Chip Layout

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