24 MPixel 36 x 24 mm^2 14 bit image sensor in 110/90 nm CMOS technology

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Abstract

We present a 35 mm film format (36 x 24 mm^2) CMOS image sensor with 6.0 µm pixels developed for digital photography. The device is manufactured with 1D reticle stitching and a 1.75 µm thin optical stack, to reduce the angular dependency of the pixel response. 14 bit counting ramp column AD converters with two counters per column are used. Power consumption at full resolution 5 fps continuous readout is 700 mW and the linear dynamic range is above 76 dB.

Process, technology and pixel design

The image sensor is manufactured at ST Microelectronics with 110 nm front-end and 90 nm copper back-end technology on 300 mm wafers. This process is originally developed for 1.75 µm pixels and has been selected for this device because of its very thin optical stack. This allows acceptance of a wide range of incoming ray angles for the 6.0 µm pixel. This is needed for compatibility to the large variety of lenses available for the camera, the wide aperture openings available on some of the optics, and the short distance between the lens exit pupil and the focal plane. The microlenses have been optimized for QE and low angular response dependency. Figure 1 shows a cross-section of the 6.0 µm pixel with the microlens and color filter. The distance between the bottom of the color filter and the photodiodes is only 1.27 µm. Figure 2 shows angular response as measured around the X axis for green light. Similar curves are obtained for the Y axis. Figure 3 shows QE, with a maximum for green light at 60%. Above 600 nm, QE is determined by the NIR cutoff filter that covers the sensor.

Chip architecture and readout path

Figure 4 shows the chip architecture. Signals from the column line pass through a PGA to a sampling stage. The PGA does a first CDS step. The gain of the PGA also reduces the noise contribution of the ADC at high gain settings. Analog and digital gain is implemented to match the camera ISO speed between ISO 200 and ISO 6400. On-chip black level offset compensation is available, using row- or frame-wise black level adjustment to measured values of on-chip optical black pixels. Row-wise offset black level compensation cancels row noise caused by noise present on common references of the PGA and the parallel AD converters. It also cancels dark current tilt in snapshot mode due to differences in integration time or top-to-bottom dark current gradients due to thermal gradients on the chip. Data is output over 7 sub-LVDS output channels running either at 125 or 250 Mbps.

Figure 5 shows the pre-amplifier stage. Adjustable analog pre-amplification is used before AD conversion with analog gain factors from x1 to x8. Lower-resolution 1080p and 720p video and window readout modes are supported, running at 30 fps with 12 bit AD conversion. For the video modes, signals from neighbour columns of the same color channel can be added together by the PGA using the Hs switches as shown in figure 5. Signals from adjacent rows can be averaged by switches Vs on the S&H capacitor banks. This summing and averaging results in lower aliasing and moiré effects in video modes.

On-chip 14 bit column counting ramp AD converters are used, which operate with a dual counter scheme per column. Figure 6 shows the counter and comparator operation and figure 7 shows the schematic. The two counters operate at opposite clock edges and count in opposite directions and at different periods of the conversion cycle. Two conversion cycles are used per row, to convert the difference between the signal level and the pre-amplifier reference level, as a second CDS step. A comparator that compares the signal level against a reference ramp waveform enables the two counters. The up counter is enabled during the first conversion cycle between the cross-point of the ramp with the reference level and the end of the cycle, and during the second cycle from the start of the cycle until the crossing of the signal level. This is similar to earlier reported operation [2]. The end value in the counter is Vsig – Vres + x, where x is an offset depending on the amount of clock cycles used in the first conversion cycle. The additional down counter, counting at the opposite clock edge, is enabled at the opposite polarity of the comparator output. Its output is Vsig – Vres –y, where y is an offset depending on the amount of clock cycles in the second conversion cycle. This dual counter scheme doubles conversion speed compared to earlier implementations ([1,2]) because both clock edges are used in the conversion process. It also ensures a continuous, signal-independent current consumption during the entire AD conversion process. At all times during the conversion cycle, exactly one counter is counting and consuming current. This avoids any data dependent IR drops which could cause row banding errors. The data from both counters is added, a fixed offset is subtracted and the data is clipped to a 14-bit word per pixel. The ADC is clocked at 250 MHz and the conversion time for one row is 50 µs. In video mode, the ADC operates with less clock cycles and converts to a 12 bit word in 17.6 µs. The resulting frame rates are 5 fps in full resolution and 30 fps in 1080p video mode.

Because pixel array dimensions exceed the reticle size, the chip is manufactured by 1D reticle stitching. The repeated pixel block is 3000 columns wide. This block also contains the column amplifiers and AD converters and is printed twice per chip.

Conclusions

Performance characteristics are summarized in table 1. Read noise is 7 e- RMS at low analog gain and reduces to 5.5 e- RMS at maximum analog gain. Full well charge is 45,000 e- , resulting in a dynamic range of 76 dB at the base gain setting.

Acknowledgement

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References

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[2] X. Wang, et al, “A 2.2M CMOS Image Sensor for High Speed Machine Vision Applications”, proc. SPIE vol. , 7536, January 2010.

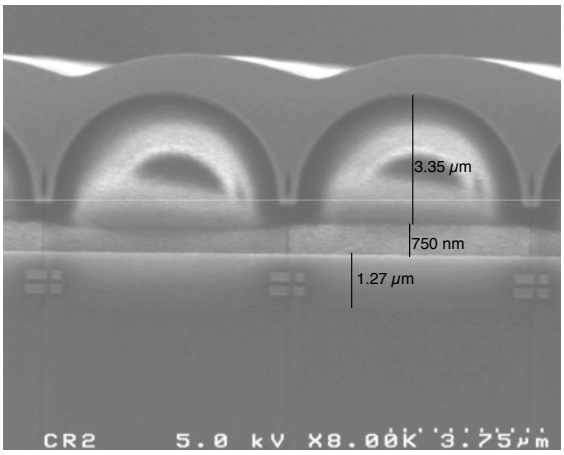

Fig. 1: pixel cross-section

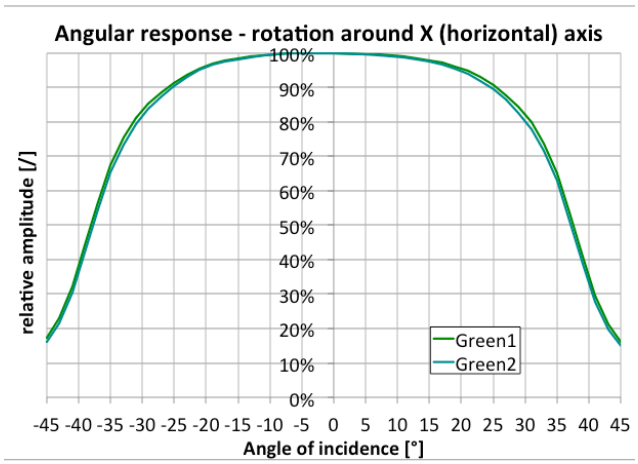

Fig. 2.: angular response

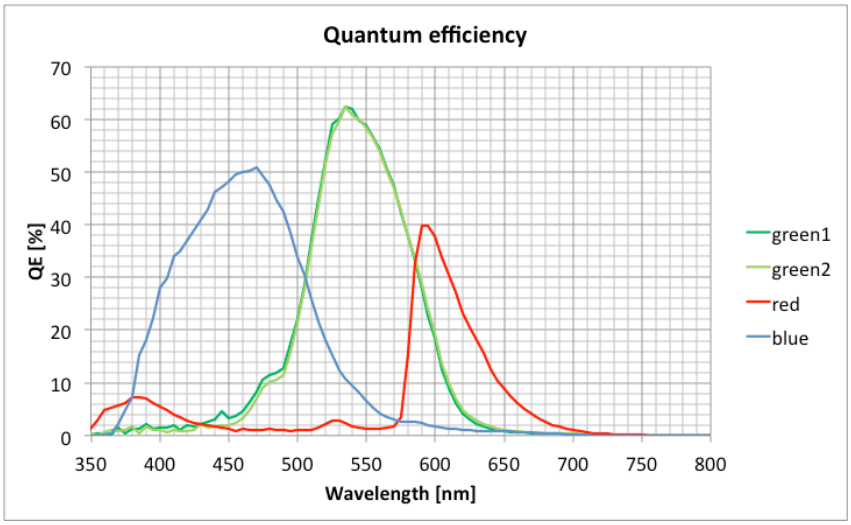

Fig. 3.: QE

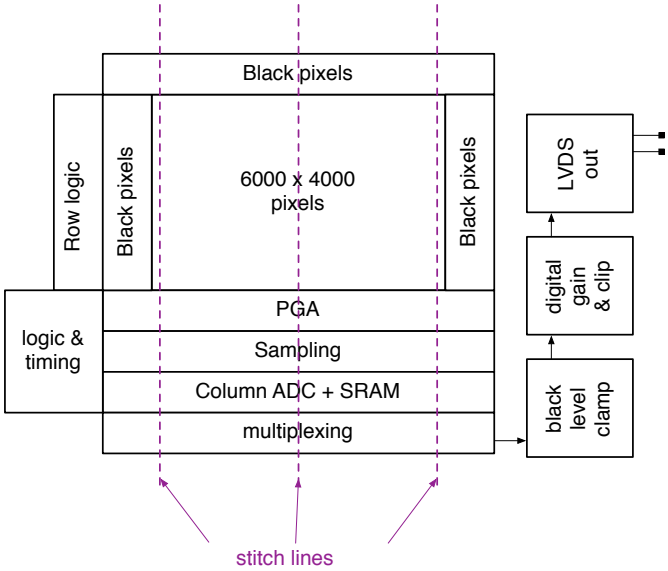

Fig. 4: block diagram

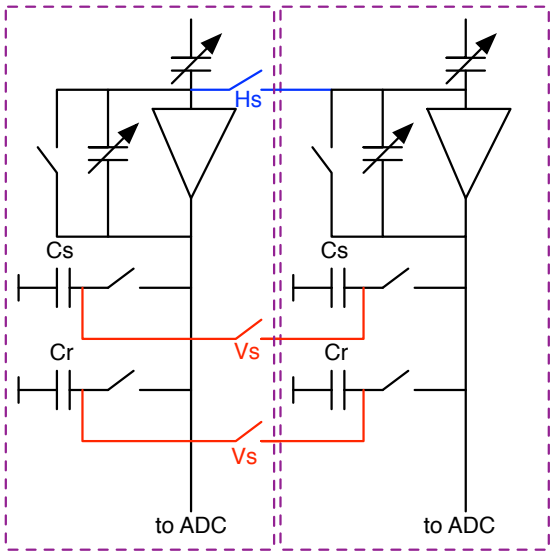

Fig. 5: column PGA and averaging

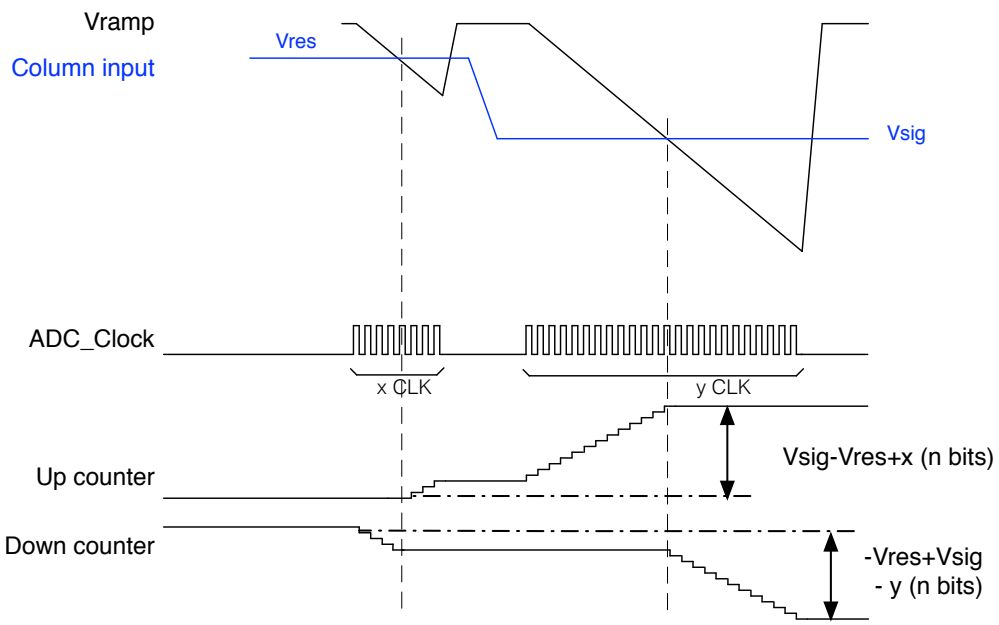

Fig. 6: ADC counting principle

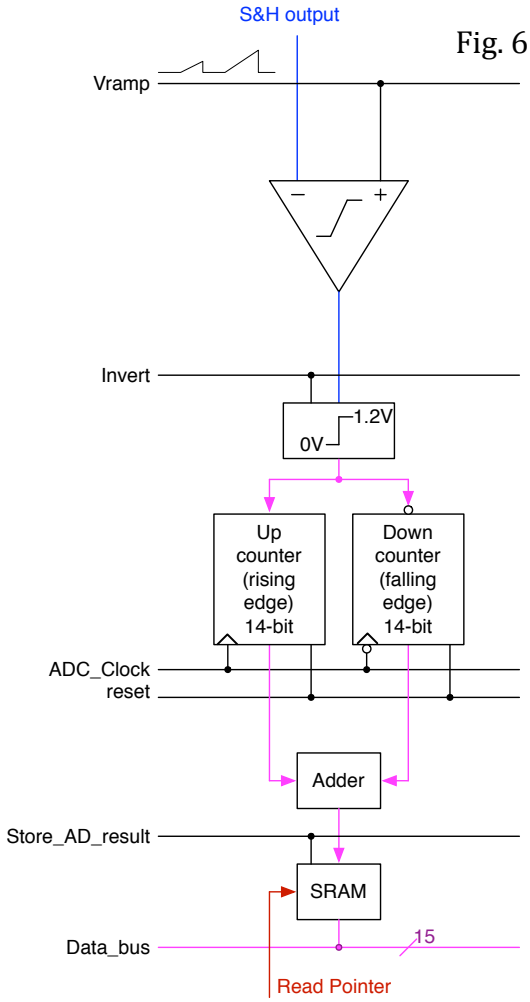

Fig.7: column ADC readout path

Parameter	Value (typical)
Full well charge	45,000 e-
Read noise (unity gain)	7 e- RMS
Read noise (+18 dB gain)	5.5 e- RMS
Dynamic range	76 dB
Pixel size	6 x 6 µm2
Resolution	6000 x 4000 pixels
Frame rate	5 fps
ADC resolution	14 bit
PRNU	1.2% RMS
QE	> 60% @ 540 nm (Green)
Dark current (25 ºC)	7 e-/s
DSNU (25 ºC)	4.5 e-/s (RMS)
Power (5 fps continuous)	700 mW

Table 1 : measured performance characteristics