

A novel architecture for the implementation of a family of high speed, multi-line CMOS image sensors

M. Moser, E. Fox, D. Deering, P. Donegan, M. Sonder, D. Marchesan, D. Verbugt, Binqiao Li, Feng-Hua Feng, Shujuan Xie, N. Safavian, R. Ghannoum, H. Mei

TELEDYNE DALSA Corporation,
605 McMurray Road, Waterloo, ON, Canada
Phone 519 886 6000, Fax 519 886 5767;
e-mail matthias.moser@teledynedalsa.com

Abstract

In this paper we describe a flexible architecture that allows for the development of a wide range of high resolution, high speed linear image sensors at minimal incremental cost per new sensor design. This architecture has been used to develop a family of image sensors for use in high speed industrial imaging. These family members differ in terms of pixel count (2k to 8k), pixel size (7 μm , 10 μm , and 14 μm), number of imaging lines (2 to 4), and effective line rate (up to 140 kHz). Select members of the family have been implemented as multi-line colour imagers for use in high end print inspection, and a quad line version has been implemented in two versions, one with enhanced luminosity sensitivity, and one targeted to applications that require R, G, B and near IR discrimination.

Introduction

CMOS image sensor (CIS) technology has been slow to displace CCD technology in high performance industrial imaging. In part, this is due to the higher development cost associated with CIS solutions. Industrial linescan applications typically require larger sensor dimensions than can be achieved with a single reticle. Stitching is commonly used to achieve the required resolutions. If properly implemented a stitched mask set can be used to manufacture sensors with different dimensions. In this development we have used a stitched architecture to develop sensors ranging from 2k pixel resolution to 8k pixel resolution [1].

Further, use of a small pitch, high bandwidth column circuit architecture followed by an analog signal mux and stand-alone serial ADCs has allowed us to develop different sensor family members in which we increase line rate and/or row count in proportion to an increase in pixel pitch. The same high net data rate is maintained across all family members independent of pixel pitch [1].

Architectural Implementation

Figure 1 illustrates the block diagram for an individual stitch slice. Each slice is configured with 2k pixels in a 7 μm pitch [1], 1.36k pixels in a 10.5 μm pitch, or 1k pixels in a 14 μm pitch. The pixel is based on a 3T-like architecture [6] in which all switching, reset, and read circuitry is located external to the pixel in order to maximize fill factor. The architecture allows for a zero spacing between pixel rows for sensors targeted to multi-line monochrome imaging [4], and a non-zero spacing for sensors targeted to multi-line colour imaging. Each column is configured with two sets of sample and hold (S&H) circuits which operate in a ping-pong fashion in order to achieve true pixel level CDS operation with maximum data throughput.

The column readout circuits are configured to multiplex two rows in parallel each through 4 signal chains per slice. In each chain the column data is multiplexed in the analog domain to a stand-alone CDS circuit to remove fixed pattern column noise, and then digitized to true 12 bit code by a stand-alone pipelined ADC. Each data chain operates at a data rate up to 50 MHz. The use of this hybrid column/stand-alone circuit architecture allows us to scale the line rate and/or the number of imaging rows in proportion to the pixel pitch. Such flexible functionality is not possible with purely column-based analog signal chains where the line rate is typically limited by the conversion time of the digitizer.

The sensor design has been implemented in a 0.35 μm , stitched, CMOS image sensor process. One of the family members that has been fabricated is a tri-linear colour sensor with a 10.5 μm pixel pitch and a 70 kHz line rate. The ability to perform full spatial sampling across all 3 colours is important for high end colour inspection application like print inspection where Moiré effects cannot be tolerated. QE curves for the red and blue pixels are plotted in Fig. 3 for the present device and for a dual line colour device that we reported on earlier [1] in which one row is composed entirely of green pixels and the second row is composed of alternating red and blue pixels. Note that the red and blue crosstalk of the TRI-linear device reaches a minimum of 1% @ 620nm.

Colour crosstalk is also minimized by spatially separating the colour rows from each other. The region between rows is configured with drains to minimize charge collection from light absorbed in these regions. However synchronization and registration requirements in the web being imaged become more challenging as the row separation is increased. Modeling was performed to optimize the selection of the row spacing. Opportunity for colour crosstalk was further minimized by arranging the individual data channels to process data from single colour rows as illustrated in Fig 2. While two of the columns support the outer row, the third column serves every other pixel of the inner row.

Another of the devices that has been fabricated is a quad-linear sensor with a 14 μm pixel pitch Fig. 4. Different colour filter array patterns have been applied to the quad-linescan device including a version with individual R, G, B, and monochrome rows, and a version with R, G, B, and IR rows for extended spectral content. Also, as illustrated by the results in Fig. 5 experiments have been performed with different starting wafer materials to optimize QE in the near IR.

A summary of the key performance specifications is captured in Table 1.

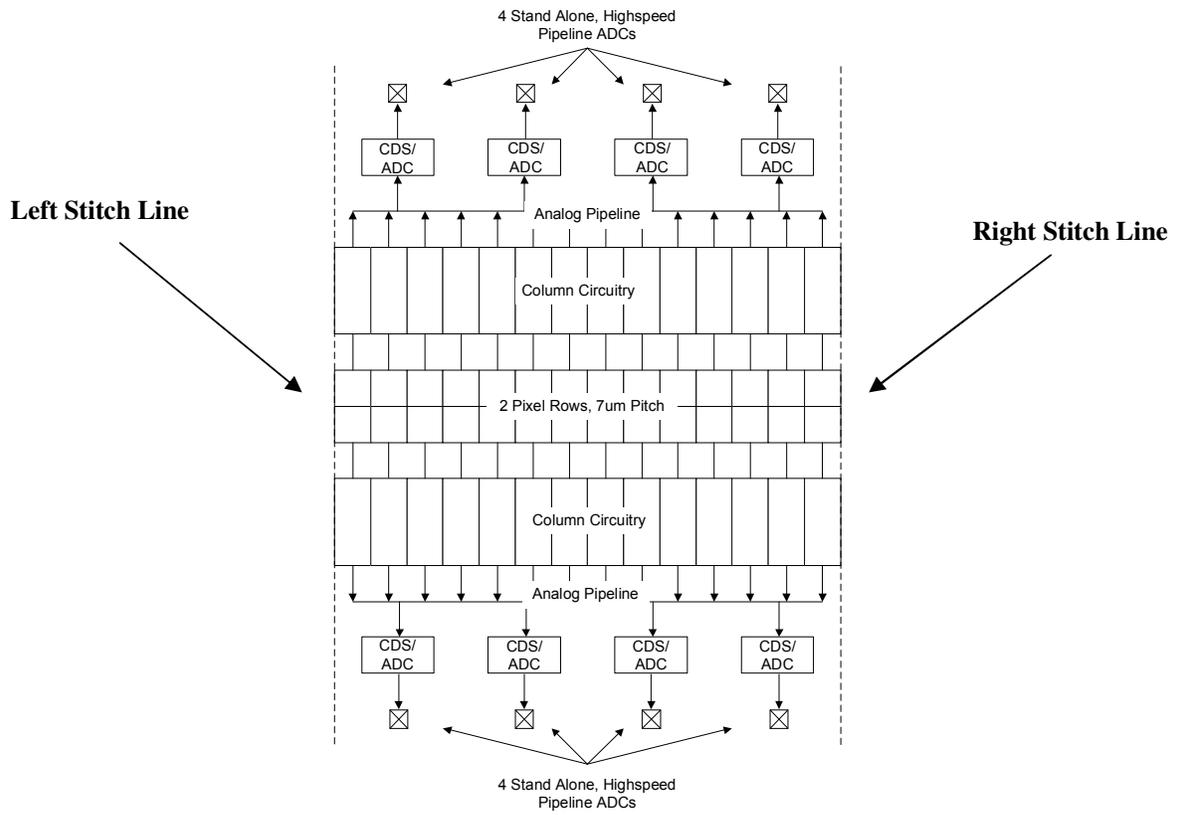


Fig. 1 – Block diagram of a single stitch slice

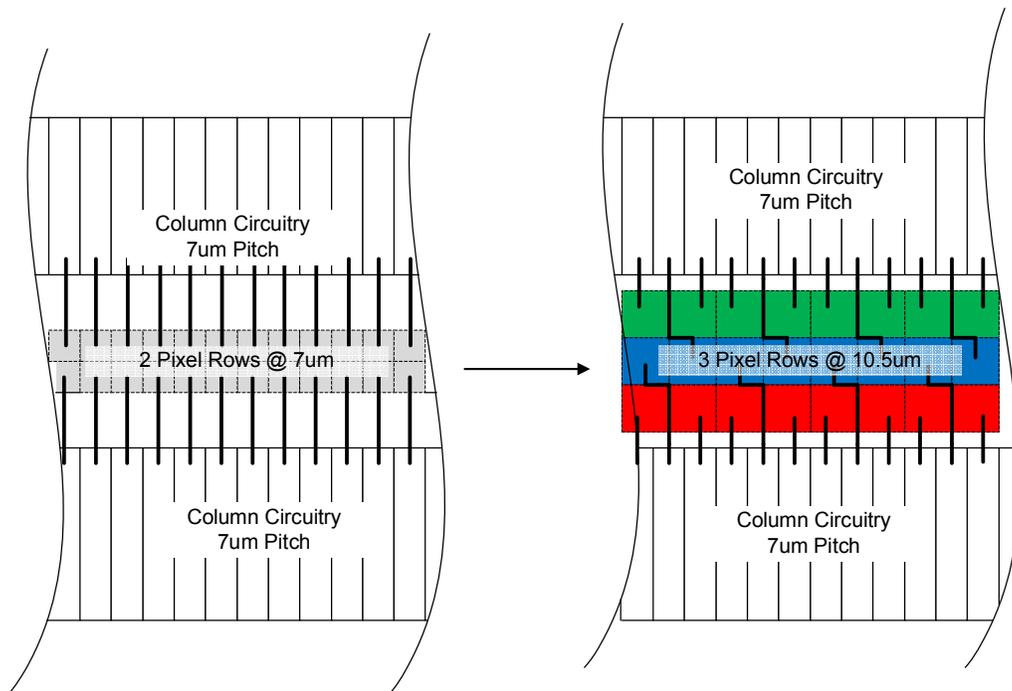


Figure 2: TRI-Linear Device, 10.5µm pixel pitch

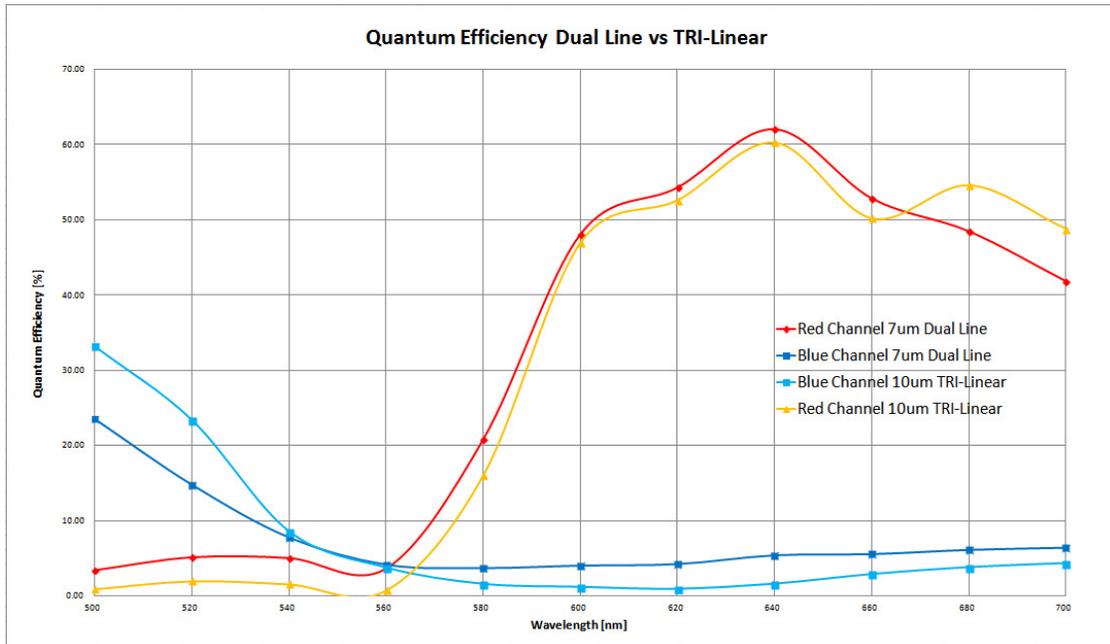


Figure 3: QE comparison, 500-700nm, Dual 7um vs TRI-Linear 10.5um

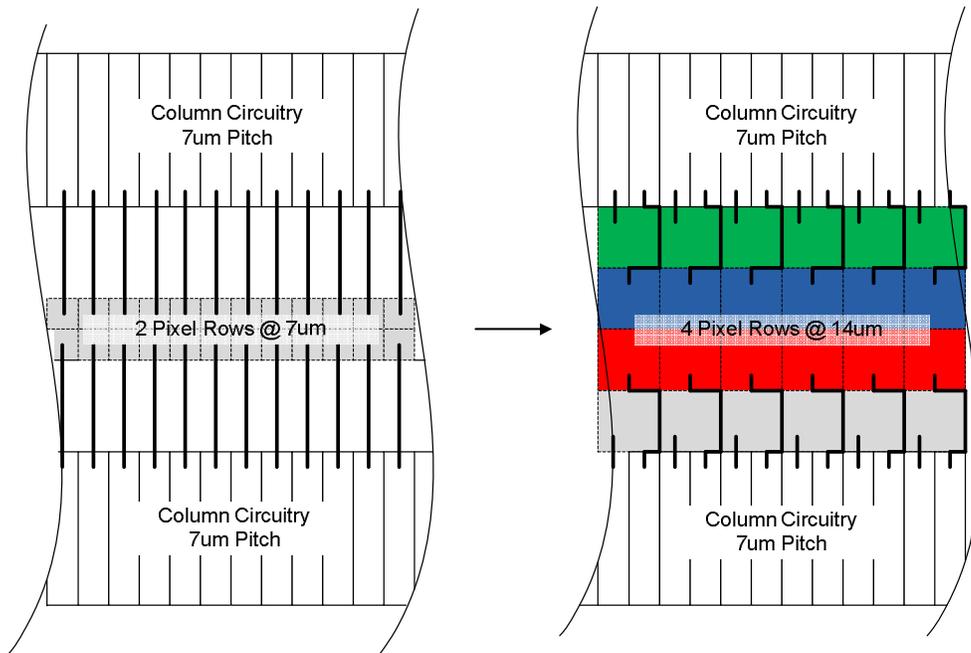


Figure 4: QUAD-Linear Device, 14um Pixel Pitch

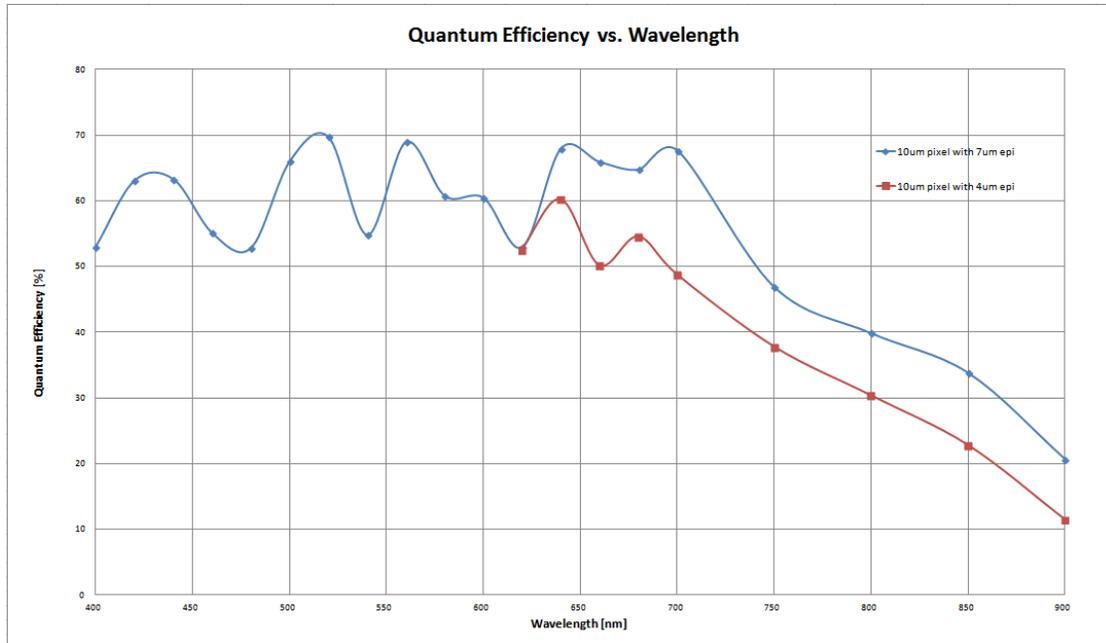


Figure 5: QE of Dual Device, 10um Pixel Pitch, 4um vs 7um epi

Sensor Performance	7um Pixel	10um Pixel	14um Pixel
Resolution	8k	4k	2k, 1k
Number of Lines	2	2 / 3	2, 4
Fill factor	100%	100%	100%
Full Well capacity	25 ke ⁻		
Conversion Gain	0.140 DN/e ⁻ per line		
Fixed Pattern Noise per channel	< 40 DN		
Photo Response Non-Uniformity	5%		
Random noise	12e ⁻		
Dynamic Range	67 dB		
Non-linearity, 10..90% saturation signal	2 %		
Line Rate	70kHz	100kHz	140kHz

Table 1: Overview of sensor performance

References

1. P. Donegan, L. Korthout, M. Moser, V. Bommu, Y. Lin, A. Kumar, F. Feng, D. Marchesan, D. Verbugt, P. Albertini, W. de Haan, S. Xie, D. Atos, W. Meas, J. de Meulmeester, M. Sonder, E. Fox, "A High Speed CMOS Dual Line Scan Imager For Industrial Applications", 2011 Intl. Image Sensor Workshop, Hokkaido, Japan
2. T. Toyama, K. Mishina, H. Tsuchiya, T. Ichikawa, H. Iwaki, Y. Gendai, H. Murakami, K. Takamiya, H. Shiroshita, Y. Muramatsu, T. Furusawa, "A 17.7 Mpixel 120 fps CMOS Image Sensor with 34.8 Gb/s Readout", 2011 ISSCC, 23-11, pp. 420-422
3. K. Yasutomi, S. Itoh, S. Kawahito, "A Two Stage Charge Transfer Active Pixel CMOS Image Sensor With Low-Noise Global Shuttering and a Dual-Shuttering Mode", IEEE Trans. Electron Devices, vol. 58, no. 3, Mar. 2011, pp. 740-747
4. G. Lepage, J. Bogaerts, G. Meynants, "Time Delay Integration in CMOS Image Sensors", IEEE Trans. Electron Devices, vol. 56, no. 11, Nov. 2009, pp. 2524-2533
5. N. O, L Wu, M. Ledgerwood, J. Nam, J. Huras, "2.5 um Pixel Linear CCD", 2007 IEEE Intl. Image Sensor Workshop, Ogunquit, USA
6. L. Korthout, D. Verbugt, J. Timpert, A. Mierop, W. de Haan, W. Maes, J. de Meulmeester, W. Muhammad, B. Dillen, H. Stoldt, I. Peters, E. Fox, "A Wafer Scale CMOS APS Imager for Medical Applications", 2009 IEEE Intl. Image Sensor Workshop, Bergen, Norway