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# Design of Analog Readout Circuitry with Front-end Multiplexing for Column Parallel Image Sensors

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## Abstract

This paper reports progress in our column parallel analog signal chain design strategy, utilizing varying degrees of parallelism for CMOS image sensors. In [1] we investigated the trade-offs for different choices of parallelism and presented an analytical model for optimization of an endoscopic sensor. We continue to use the analytical model and have developed an improved analog readout circuitry that has enabled us to reduced silicon area, achieve higher frame rates, while improving SNR performance. The design is highly scalable and has been implemented in both a high-resolution large format sensor at 60FPS and a lower-resolution small form factor sensor at 600FPS. It features a fully differential readout with a high-speed redundant successive approximation A/D converter (SAR-ADC). The analog readout circuitry presented here was tested in a prototype sensor fabricated in 0.18um 3.3V/1.8V CMOS process. The measured results from the prototype sensor shows the signal chain achieving 248uV input referred noise with a throughput of 17.5Mpixel/sec while consuming an estimated 126uW per pixel column.

## Introduction

Design of analog readout circuitry for CMOS image sensors continues to face challenges in achieving high speed, small area, low power, and low noise. We are faced with continual shrinkage of pixel size with increasing requirements on resolution and frame rate. Recent trends for achieving high dynamic range images with multiple high/low exposures reads is also pushing the effective readout rates higher even when the sensor's effective frame rate remains the same. Confronted with these design parameters of competing criteria, we continue to rely on our analytical model to optimize the degree of parallelism in our analog readout circuit.

In this paper, we present an improved analog readout circuit [1] designed in combination with our analytical model to find the optimal degree of parallelism. The improved design is fully differential with a high-speed Successive Approximation (SAR) ADC. The design increases the achievable SNR while reducing supply voltage requirement thus lowering the overall power consumption.

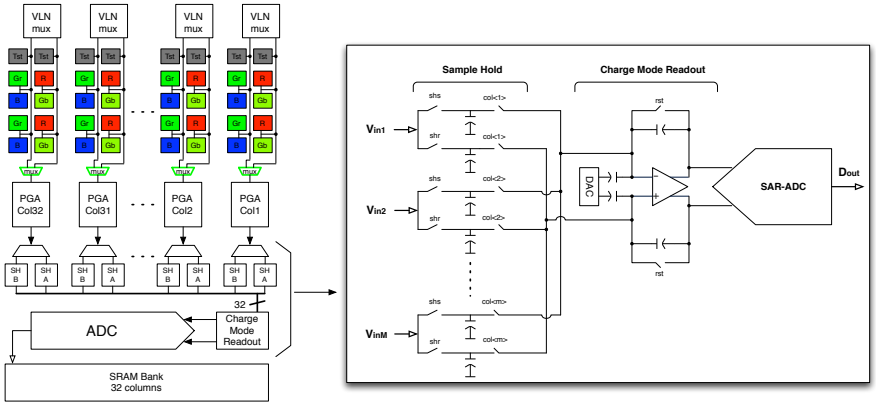


Figure 1: Readout Floor Plan and Block Diagram

Figure 1 shows the block diagram of the analog readout circuit. It consists of an array of 32 dual bank sample and hold capacitors followed by the charge mode readout circuit. The charge mode readout stage functions as a level shifter to convert the sample and hold signal to fully differential and as a buffer to drive the signal into the differential SAR-ADC. Data is written back into a dual bank SRAM storing the 32 columns of data for readout.

**Model Application**

At the onset of the sensor design project, we apply our analytical model to the sensor specification requirements. In this study phase, we design the sensor architecture at the top level estimating the area, noise, power and speed of the readout chain. Using our model, we identified a value M that meets our constraints while maintaining the sensor frame rate. The model results are plotted in Figure 2. M=32 was selected as a result of our design trade for lower area and power consumption.

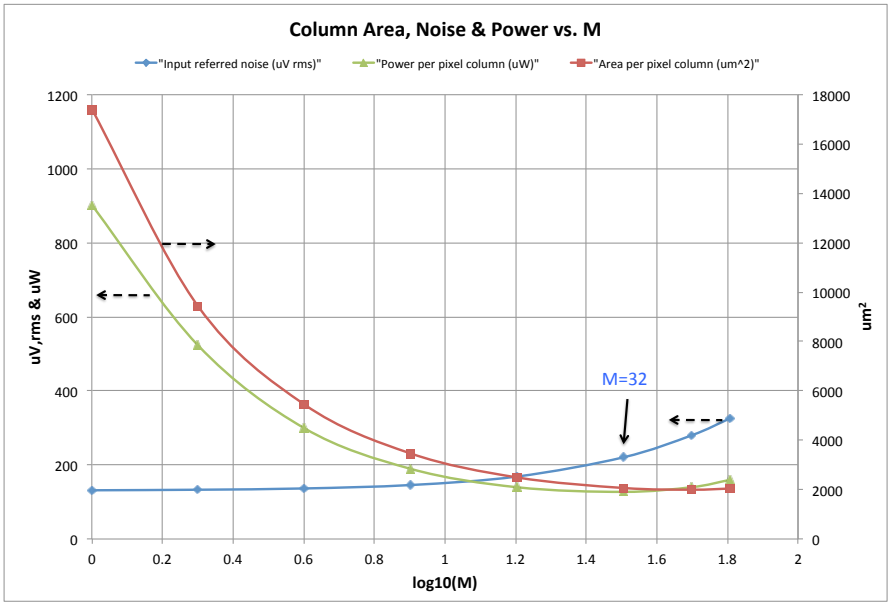


Figure 2. Analytical Model for Trade-off

**Charge Mode Readout Circuit**

The charge mode readout stage shown in figure 1 reads out each pixel column's signal differentially through the charge domain [2]. Simultaneous with the column selection, there is a level shifting DAC that is enabled during readout to shift the output voltage to the desired level through the summing node of the amplifier. As a result, the output voltage swings differentially from -1V to +1V centered on the common mode level. With the fully differential signaling, the buffer amplifier can now be designed with a 1.8V supply while still outputting 2V peak-to-peak. The buffer amplifier designed is shown in Figure 3. The topology chosen is a two-stage amplifier with a folded cascode first stage followed by a common source second stage. The second stage topology was chosen to achieve maximum output swing for a given supply voltage.

Timing between the charge mode readout and the ADC conversion is shown in Figure 4. The readout rate for the data path is design for 17.5Msample/sec. This readout period is split between the buffer amplifier driving the column signal into the ADC and the SAR ADC taking 14 clock cycles to perform a conversion. A high-speed 280MHz clock is distributed across the sensor array while all other timing control signals are generated locally. Having local timing

generations allows each readout block to operate independently and therefore the propagation delay of the high-speed clock is not a factor for scaling the number of parallel blocks for large arrays.

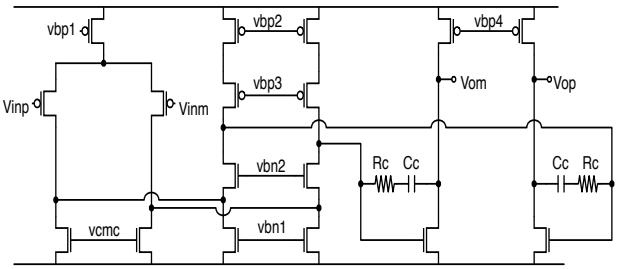


Figure3. Charge Mode Readout Amplifier

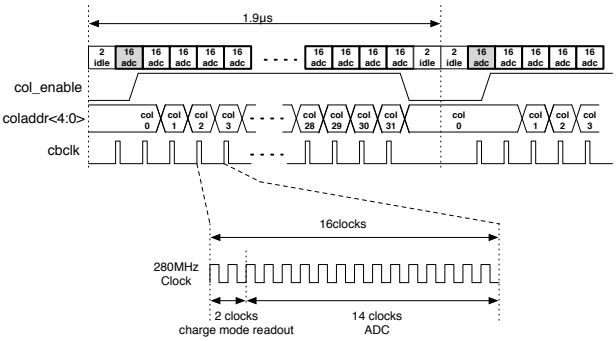


Figure 4. Readout Timing

**Redundant SAR ADC**

One of the main factors limiting the conversion rate for SAR ADC is the time taken to settle the reference voltage. It is especially crucial in applications such as column parallel ADCs where there is an array of ADCs sharing a common reference voltage. Techniques such as sub-radix 2 SAR ADC [3] have shown that the reference setting requirement can be greatly relaxed thru redundancy in the output codes. Applying this technique, we can speed up the ADC conversion rate to a point where the references only need to settle to within the digital redundancy region.

Figure 4 shows a simplified block diagram of the SAR-ADC. The ADC adopts a fully differential radix-1.85 architecture. The radix was chosen based on capacitor matching, reference settling accuracy, and conversion rate parameters. By choosing a lower radix, this increases the digital redundancy region and therefore relaxes the reference settling. However the trade-off is increased requirement on capacitor matching to achieve the desired bit resolution.

Minimizing the capacitor sizing is critical not only to reducing reference settling but also for lowering the required area and reducing the power consumption of the buffer amplifier driving the input. Sizing of the capacitor is determined mostly for matching requirement for a given resolution. Having the SAR capacitors scale in a non-binary radix also complicates the layout and matching of the unit capacitor. To help alleviate these requirements, we applied two techniques. First we split the array into two-halves with separate reference voltage. Second to compensate for reference voltage and capacitor mismatch we implement a foreground calibration [3] to calibrate the effective weight of each capacitor. The result of these techniques enabled us to reduce the total capacitance size to 0.7pF which is a manageable size for our requirements.

**Conclusion**

A prototype high-speed, column-parallel image sensor was designed with the analog readout circuit architecture and fabricated in a 0.18 um 3.3V/1.8V CMOS process. Analog test inputs were used to inject a known analog input voltage and to characterize the readout. The measured DNL and INL performance of a typical ADC within the array is shown in Figure 6. The foreground calibration shows improvements mostly to the INL of the ADC to compensate for reference voltage and capacitor mismatch. The measured input referred noise is shown in Figure 7.

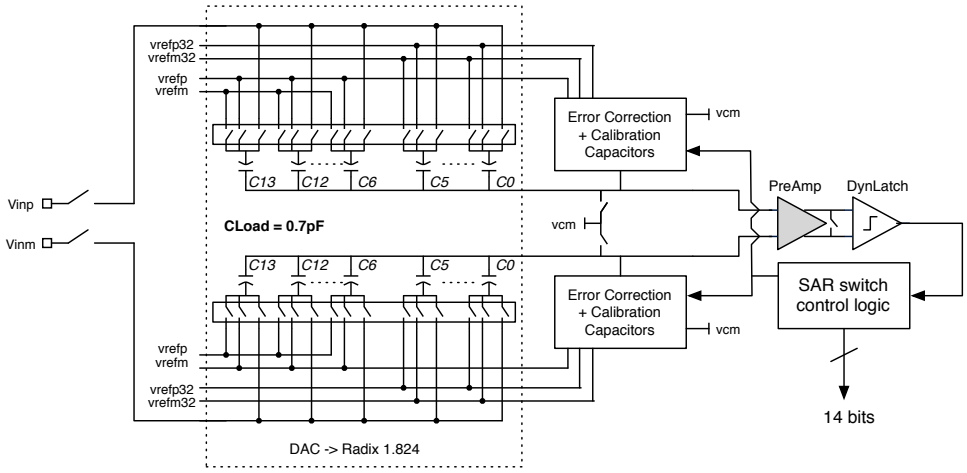


Figure 5. Sub-Radix2 SAR-ADC

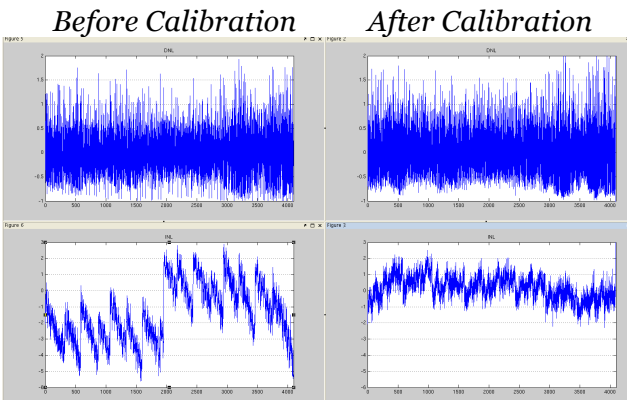


Figure 6. DNL INL Measurement

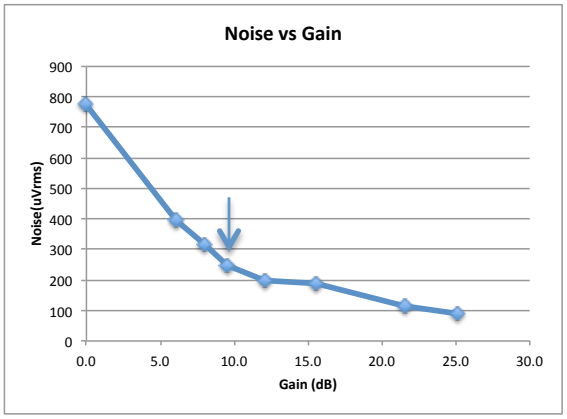


Figure 7. Analog Chain Noise

**Acknowledgment**
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**References:**

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[2] A. Krymski, "Charge domain analog readout for image sensor," U.S. Patent 6 222 175, Apr. 24, 2001.
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