

# Digital Integration Sensor

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**Abstract**—Analytical and experimental results with the Digital Integration Sensor (DIS) imaging concept, including dynamic range extension, are reported in this paper. The “quantized” DIS (qDIS) concept is proposed. The continuum between the conventional CMOS APS, the DIS, the qDIS and the QIS is discussed as a sort of roadmap, along with trades in power and performance enhancement.

## I. INTRODUCTION

Most image sensors work in charge-integration mode. Photoelectrons accumulate and are stored in the pixel before final read-out operation. As pixels shrink, full well capacity of the pixel decreases. To collect enough signal charge and maintain SNR, digital integration could be used [1-4].

In the Digital Integration Sensor (DIS), as shown in Fig. 1, the original integration period is divided into several subintervals or fields. Each pixel is reset at the beginning or during each subinterval. At the end of each subinterval, integrated signal charge is read out. The signal is then digitized and integrated in digital memory. One frame of digital memory is often already used in camera systems, although in the DIS the memory is used prior to ISP.

## II. SENSITIVITY VS. DYNAMIC RANGE

DIS is a promising way to solve the well-known conflict between sensitivity and dynamic range.

As signal charge is read out (as  $V_{sig}$ ) multiple times during the original integration period, less charge needs to be stored in the pixel. The full-well capacity can be intentionally decreased without jeopardizing dynamic range. In turn, that allows higher conversion gain, thus lower input-referred read noise. Although total read noise would accrue due to multiple read-out operations, it is balanced out by higher conversion gain and the sensor could still achieve better read noise performance.

For example, say conversion gain is increased by a factor of  $n$ , and  $m$  fields are read out and summed to form a single image. To get more general results, we assume that  $m$  doesn't have to be equal to  $n$ , but we should note that the inequality may lead to different total integration time. Table 1 shows a performance comparison between DIS and SOA CMOS APS.  $V_n$  is output-referred read noise level (rms).  $V_{sat}$  is the saturation value of  $V_{sig}$ .

To make sure that both input-referred read noise and maximum signal capacity of the DIS show no worse performance than SOA CMOS APS,  $n$  and  $m$  should obey the following relation:

$$n \leq m \leq n^2 \quad (1)$$

Another noteworthy result shown in the table is the improvement of dynamic range which only depends on the value of  $m$ .

If the total integration time is  $T$  and cannot be exceeded,  $n$  should be equal to  $m$ . Maximum signal

capacity is exactly compensated to the same value while input-referred noise is improved by  $20\log(\sqrt{n})$  dB. Alternatively, this improvement provides a margin in read noise requirement. This margin could be traded for other aspects of performance of read-out circuits, such as speed and power consumption.

ADC resolution requirements are reduced due to multiple reads. For example, say the full-well capacity of the pinned photodiode is reduced from 4000 to 1000 e-rms. This allows smaller pixel pitch including the FD. The conversion gain might be increased 4x to reduce read noise, and the ADC resolution can be reduced by 2 bits, easing ADC design and power and/or increasing ADC speed. However, writing digital data to memory at higher field rates will add to total system power dissipation.

## III. DIS AS HDR IMAGE SENSOR

Since multiple fields are needed for the DIS, it was proposed that the integration time of each field be varied to increase the dynamic range of the sensor [3]. This is similar to one of the methods used to improve DR in conventional sensors [5-8].

The full-well capacity limits the signal charge that could be integrated during certain amount of time. So the essence of HDR image sensor design is to use this limited range of signal charge to represent larger light intensity range. This could be achieved by introducing nonlinear response between light intensity and signal charge instead of linear response, e.g., logarithmic response [9].

By varying the integration time of each subinterval, DIS shows a nonlinear piecewise response curve, as shown in Fig. 2. The maximum detectable light intensity is extended to a higher value. At the same time, the minimum detectable light intensity decreases due to lower read-out noise. Total enhancement in dynamic range is:

$$\Delta DR = 20\log\left(\frac{\sqrt{n} \cdot \bar{T}}{T_n}\right) \quad (2)$$

where  $\bar{T}$  is  $1/n$  of total integration time and  $T_n$  is the shortest subinterval.

High dynamic range comes at the cost of SNR. This is because less signal charge is used to represent a change in high light intensity. Fig. 3 shows an example of theoretical SNR curve for DIS as an HDR image sensor. Maximizing SNR while minimizing any dips in the curve is part of HDR optimization.

An experiment using a Canon 60D DSLR was conducted to verify this idea. Fig. 4 shows that dynamic range is extended to over 88 dB using just 8b from camera output for each of 16 fields, each of varying exposure time, which compares to 60 dB for 14b ADC single shot with same total exposure time in normal operation. DR is determined using Airy disk pattern methodology as described in [10].

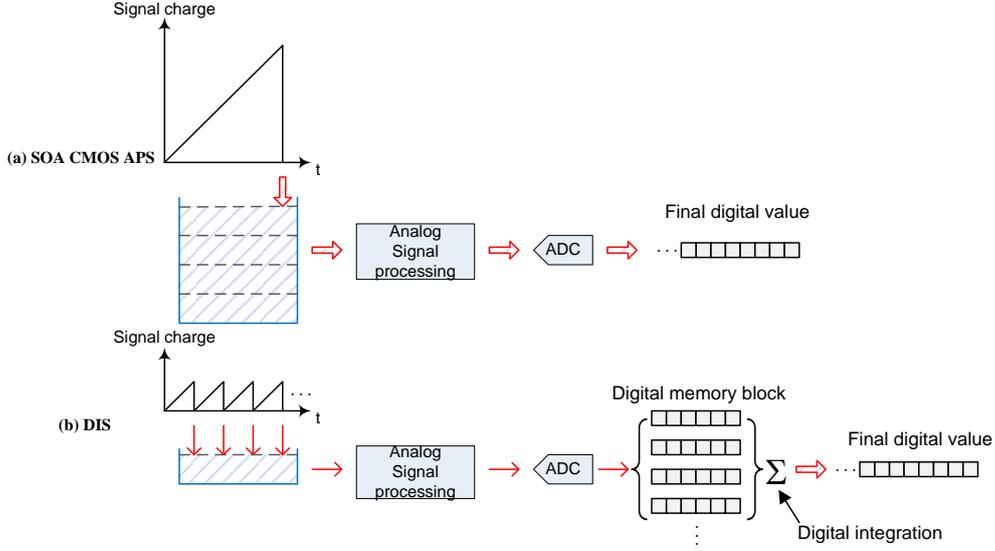


Fig. 1. Illustration of DIS concept comparing to SOA CMOS APS

Table 1. Performance comparison between DIS and SOA CMOS APS

	Conversion gain	Input-referred read noise (RMS) /e <sup>-</sup>	Maximum Signal Capacity /e <sup>-</sup>	Dynamic Range	Total integration time
<b>SOA CMOS APS</b>	$C.G.$	$\frac{V_n}{A_v \cdot C.G.}$	$\frac{V_{sat}}{A_v \cdot C.G.}$	$\frac{V_{sat}}{V_n}$	$T$
<b>DIS</b>	$n \cdot C.G.$	$\frac{\sqrt{m}}{n} \cdot \frac{V_n}{A_v \cdot C.G.}$	$\frac{m}{n} \cdot \frac{V_{sat}}{A_v \cdot C.G.}$	$\sqrt{m} \cdot \frac{V_{sat}}{V_n}$	$\frac{m}{n} T$
<b>Improvement (dB)</b>	$20\log(n)$	$20\log\left(\frac{n}{\sqrt{m}}\right)$	$20\log\left(\frac{m}{n}\right)$	$20\log(\sqrt{m})$	N/A

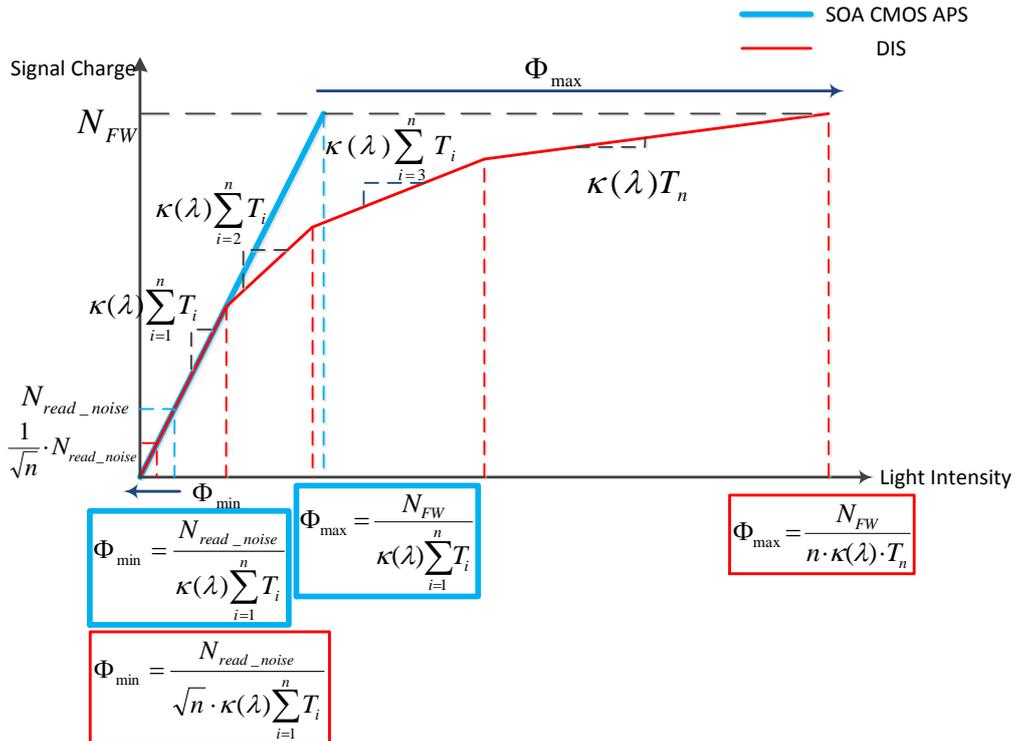


Fig. 2. Signal charge vs. light intensity response curve of DIS and SOA CMOS APS

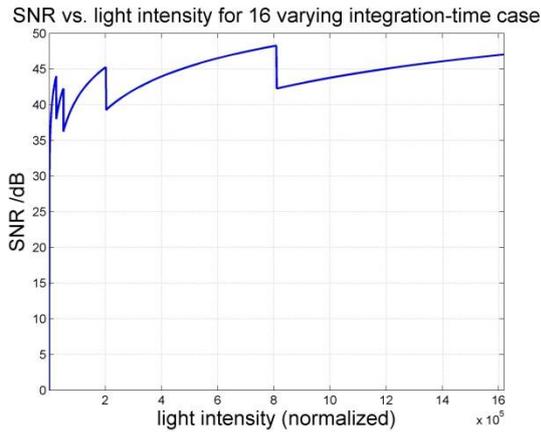


Fig. 3. An example SNR curve for DIS

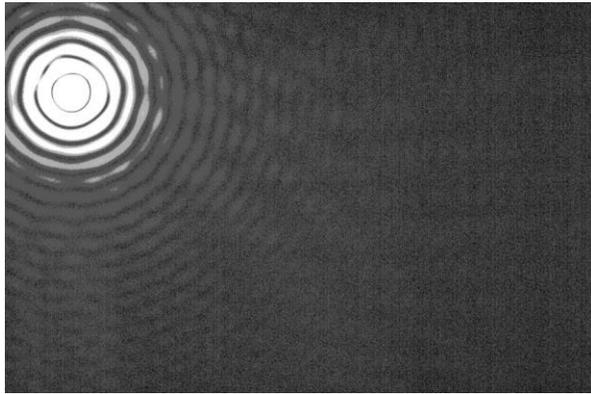


Fig. 4. Experiment result on DIS as HDR image sensor

#### IV. qDIS

If we increase the conversion gain more aggressively, the read noise could become so low as to allow discrete electrons to be sensed such that the output of the pixel is in discrete levels, each corresponding to a different number of electrons. This is the “quantized” DIS (qDIS) concept. The ADC quantization could be made to correspond to the number of electrons in the FD. For example, a 4b ADC code of 0101 would mean 5 electrons in the FD. The Bit Error Rate (BER) of the ADC code has a strong dependence on  $V_n$ . Fig. 5. shows how to calculate BER from the probability distribution of  $V_{sig}$  for a given  $V_n$ . The relation between read noise level and BER [11] is shown in Fig. 6.

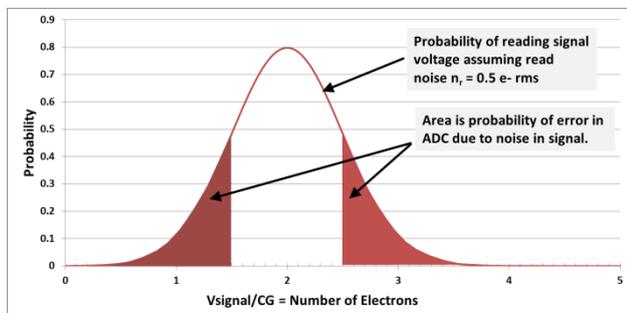


Fig. 5. Illustration of how bit error rate (BER) is determined by noise before the quantizer. A read noise of 0.5 e- rms is chosen to make the illustration easier.

To achieve a low bit error rate, the qDIS would likely need a read noise under 0.15 e- rms and CG above 1mV/e-. This leads to a full well of perhaps 128 e- and 32

fields of digital integration for a linear DR of  $20 \log(4096/0.15/\sqrt{32}) = 74$  dB. Having the same read noise requirement as for the QIS is not surprising since discriminating between one electron and none is nearly the same problem as discriminating between, say, 23 and 24 electrons, except one needs more bits in the ADC, and INL and DNL well below one LSB.

The histogram density of pixels with value  $V_{sig}/CG$  for exposure  $H$ , where  $CG$  is the conversion gain, is given by:

$$N_{pixels}(V_{sig}/CG) = \sum_{k=0}^{\infty} \frac{1}{V_n \sqrt{2\pi}} \exp\left[-\frac{(V_{sig}/CG - k)^2}{2V_n^2}\right] \cdot \frac{e^{-H} H^k}{k!} \quad (9)$$

where the first multiplicand is the read signal distribution due to read noise, and the second is the probability of  $k$  photons arriving at a pixel for exposure  $H$ . This is shown below in Fig. 7.

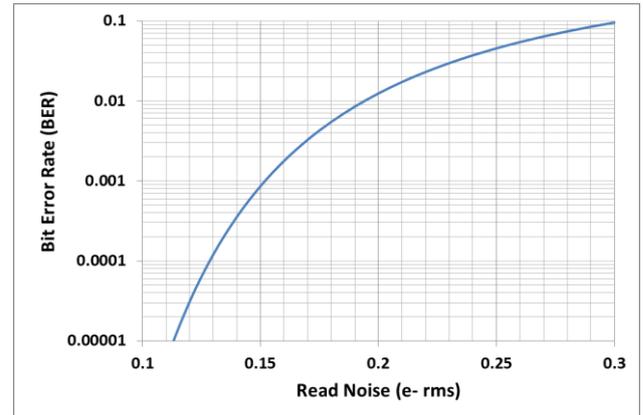


Fig. 6. Strong dependence of BER on read noise in the qDIS. Read noise should probably be below 0.15 e- rms

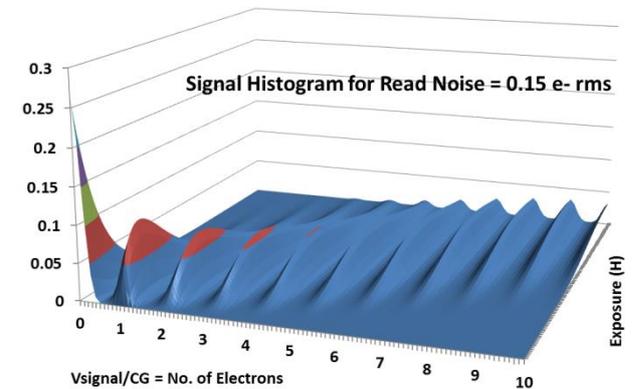


Fig. 7. qDIS histogram of  $V_{sig}$  (divided by conversion gain  $CG$ ) for quanta exposures from 0-10 photoelectrons per pixel.

#### V. ROADMAP FOR DIS, qDIS, QIS

From DIS to qDIS to QIS [12], we are approaching the quantum nature of signal charge. In DIS, we mitigate the conflict between sensitivity and DR. Reduction of read noise can be achieved from higher conversion gain. In qDIS, though its read-out architecture is still based on analog circuits and ADCs, read noise would be at such low level that it makes photoelectron counting possible with a relatively low BER. In QIS, each signal charge could be directly sensed as a binary-valued signal. Table 2 gives an estimate on how the detailed parameters would evolve from DIS to qDIS to QIS.

## VI. ACKNOWLEDGMENT

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Table 2. Conventional CMOS APS compared with DIS, qDIS and QIS. Values are illustrative only.

	CMOS APS	DIS	qDIS	QIS
Pixel Size (um)	40-1.1	1.4-0.2	1.4-0.2	0.5-0.1
Photosites per sensor	10k-100M 8-12M typ.	12M-100M	12M-100M	100M-100G
Output rate (pix/s)	1M-8G	10M-10G	10M-100G	10G-10T
Output rate (b/s)	10M-100G	100M-100G	100M-100G	10G-10T
Full well capacity (e-)	100,000-3,000	4,000-200	1,024-8	1
Conversion gain (uV/e-)	50-150	100-200	1,000-10,000	1,000-10,000
Read noise level (e- rms)	1-5	0.2-5	<0.15	<0.15
Photoelectron Counting	N	N	Y	Y
ADC (b)	10-14	6-10	3-10	1
Fields/Frame	1-2	4-32	4-1,024	8-64
Reads/Pixel	1-2	4-32	4-1,024	256-65,000