Designing Incremental Sigma-Delta ADCs for low Thermal Noise in Image Sensors

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***Abstract*—Incremental Sigma-Delta (ISD) ADCs are becoming popular in the imaging field mainly due to 2 characteristics: the intrinsic oversampling of the converter which decreases the thermal noise of the pixel source follower and the reduced accuracy required by the analog building blocks. In this paper we present some design guidelines for choosing the appropriate ISD architecture according to the imager design specifications in terms of conversion speed, power consumption and noise. Furthermore, we propose some novel solutions to common ISD design issues, such as modulator reference buffering, which hinder the implementation of this converter type in high speed, high resolution image sensors.**

Keywords—Incremental Sigma Delta, ADC, low noise, low power, shared opamp, reference buffering, calibration

I. INTRODUCTION

Recent trends in imaging applications require high dynamic range and high spatial resolution at higher frame rates demanding high performance column level ADCs. Given their intrinsic oversampling feature, ISD ADCs [1] [2] are appealing in the imaging field due to their ability to reduce the pixel source follower (SF) thermal noise, and their ease in reaching high resolution (e.g. >14bit) with relatively low precision analog components. In this work we will address some key issues of this ADC architecture such as power and area consumption together with implementation difficulties in high resolution, high speed imagers due to the need for fast reference voltage buffering.

This paper is organized as follows: in section II we guide the reader through the most important choices to make with respect to modulator topologies and opamps. In section III we propose specific solutions for improving crucial characteristics such as power and area consumption and we introduce a column specific buffering system with calibration to be used in high resolution, high speed arrays. Finally, conclusions are drawn in section IV.

II. GENERAL DESIGN GUIDELINE FOR MODULATORS

A. Topologies

ISD ADCs are composed of a modulator converting the analog input into a bit stream and a digital filter converting the bit stream into the binary representation of the analog signal. Typical modulators are composed of integrators, a quantizer and a DAC. The most common modulator topologies are the Feed-Forward (FF) and the Feed-Back (FB) as shown in Fig. 1. The FF architecture has the benefit of a reduced integrator output voltage swing [3], allowing the use of low output voltage swing, low-power operational trans-impedance amplifiers (OTA) such as telescopic or cascoded common source [4]. Hence, the FF architecture is the most appealing topology in column-level ADC implementations.

In order to facilitate the column-level power supply distribution and to limit the ADC area, a low-order modulator, typically 2^{nd} (mod2) or 3^{rd} (mod3) with single bit quantizer is preferred. The choice between the two is a matter of conversion speed, power, noise and area. In terms of conversion speed, mod3 outperforms mod2. For example, a 16-bit conversion requires 381 samples for mod2 and 127 samples for mod3 [5], which is three times less samples for the same resolution. Mod3 is, however, also more prone to instability.

Mod2 usually consumes much less area and, in some cases, less power than mod3. Omitting for simplicity the cycle-dependent weight coefficients of the digital filters [2], using 3 times more samples and therefore improving the thermal noise averaging, translates into a 3 times smaller mod2 sampling capacitance. Moreover, the number of integrators is reduced by 1 unit, fewer switches are used and the digital filter is an order smaller.

The capacitors and OTAs consume most of the area of the modulator. The optimal modulator coefficients of mod2 and mod3 [3], indicate that, to first approximation, mod2 uses a 2.6 times lower capacitance area.

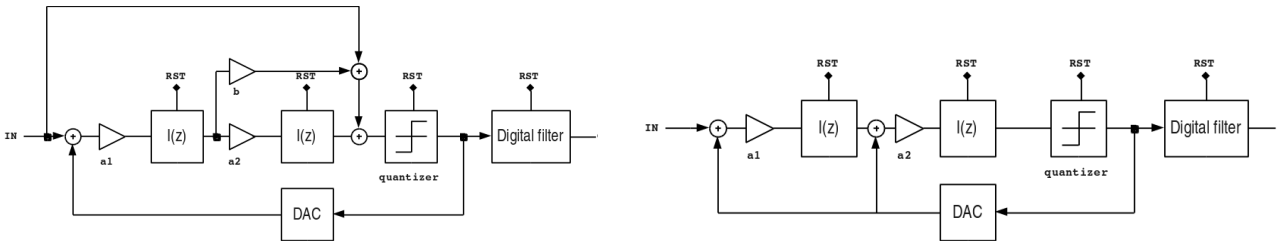


Fig.1. Feed-Forward (a)) and Feed-Back (b)) second order ISD ADCs. The integrators, the quantizer and the digital filter have a reset switch which is activated after each analog-to-digital conversion.

B. Operational amplifier

The OTAs are the most power consuming building blocks of the ISD ADC [3]. The main specifications of the OTAs in a modulator are DC gain, gain bandwidth and noise. In order to evaluate the values for these parameters, extensive behavioral simulations are needed.

In order to lower the power consumption, [2] proposes the use of inverters as amplifiers. This solution is very appealing, especially in terms of area consumption. However, due to the nature of the inverters, the current consumption is highly dependent on process variations, making the power consumption of the inverter-based amplifiers unpredictable.

Common source cascode amplifiers (Fig. 2 a)) is another conventional architecture used in previous works [4]. Similarly to the inverter-based amplifier, they suffer from reduced power supply rejection ratio (PSRR).

The telescopic cascode architecture (Fig. 2 b)) provides high gain due to the increased output impedance by stacking more transistors i.e. cascoding. The decreased output voltage swing of this architecture is mitigated by the use of a FF modulator architecture. Its good PSRR and the common mode voltage control, make the telescopic OTA a reasonable choice for column level ADC implementation.

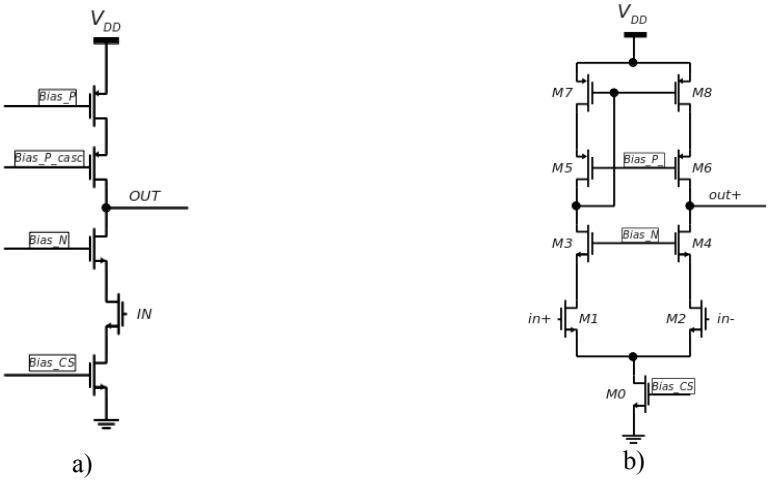


Fig.2. Common source cascode (b)) and telescopic cascode (b)) OTA architectures

III. GUIDELINE FOR IMPROVING SPECIFIC FEATURES

A. Power and area reduction

In order to decrease the area and the power of the ADC, a feed-forward, second-order modulator with shared-OTA is proposed. This technique is based on the fact that the integrators of the modulator have 2 phases: sampling and amplifying. The OTA is used only at the amplifying phase and it drowns unnecessary current during the sampling phase. Fig. 3 shows a FF mod2 with half-delay clocks needed for the shared-OTA implementation. While the first integrator works in sampling phase, the second integrator works in the amplifying phase. One OTA can, therefore, be shared by the two integrators by rearranging the switches and the capacitors. Fig. 4 b) shows the circuit level implementation of the proposed modulator which, compared to the conventional FF mod2, eliminates the second OTA, sparing area and reducing the power consumption by 20%.

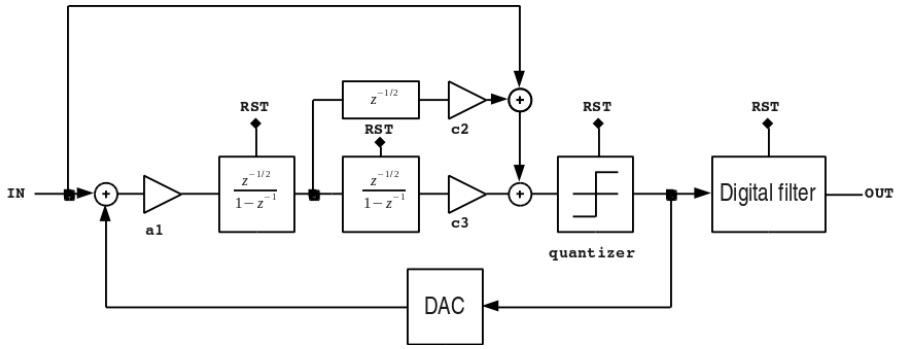


Fig.3. Modified second-order Feed-Forward structure for half delay implementation

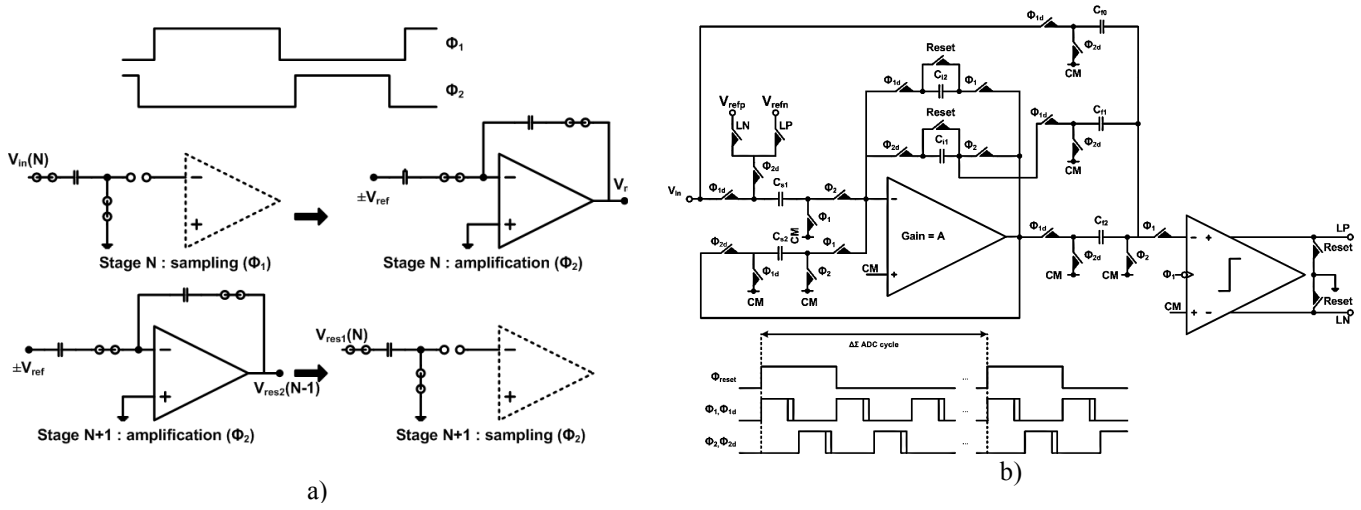
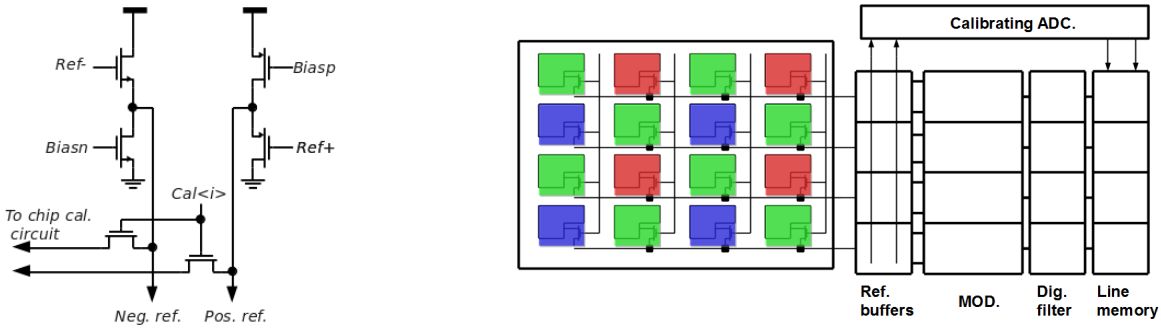


Fig.4. a) OTA sharing technique: stage N samples at Φ1 while stage 2 samples at Φ2. A single OTA is used in both phases: amplifying stage N at Φ2 and amplifying stage N+1 at Φ1. b) Proposed single OTA schematic: the area and the power of the second OTA consumed in the standard FF architecture are eliminated by the proposed technique.

B. Reference buffering for high speed, high resolution arrays

In order to implement the single bit DAC function in the modulator, 2 reference voltages are required. On-chip buffers are typically employed to drive the same reference voltages to all the modulators in the columns. Driving multiple columns with a single buffer is challenging in case of high switching speed and/or multi-column array. Chip-level buffers can consume an important fraction of the power budget of the imager. Although column-level, source-follower-based buffers could be more power efficient, they introduce gain vertical pattern noise (GVPN) due to the threshold voltage variations of the SFs, requiring calibration.

In this paper we propose a column-level SF-based reference buffer with a background calibration technique for ISD ADCs. Fig. 5 a) shows the schematic of the reference buffer with select transistors used to connect the output of the SF buffers to the calibration block. An added on-chip ISD (e.g. an extra column ADC) sequentially converts the reference voltages of the column buffers in the background without image capturing interruption and does not impact the frame rate of the imager. The digitized references are then stored in a second line memory (Fig. 5 b)). The digitized pixel value is multiplied to the digitized reference value right before the digital I/O operation providing GVPN free information. In addition, the reference voltage deviations due to temperature variations are also calibrated.



a) b)

Fig.5. a) Column-based reference voltage buffer with an NMOS source follower for negative reference and a PMOS based one for positive reference. This allows a power consumption reduction over the chip-level buffer at the cost of increased vertical pattern noise. b) Background buffer reference calibration: the added chip-level ADC sequentially converts the reference voltages at the output of the column buffers and updates a second line memory of the ADC. No frame capturing stop is required to perform the calibration.

IV. CONCLUSIONS

In this paper we showed some design guidelines for choosing the appropriate modulator topology according to the ADC performance specifications. The FF modulator generally performs better than the FB due to the reduced output swing of the integrators, allowing the use of low power, low voltage OTAs. Mod2 is preferred to mod3 in case noise and area are the most stringent specifications while the implementation of mod3 is advised when a very high conversion speed is required. In order to decrease the area and power of the ADCs we introduced a FF mod2 with shared-OTA which allows to spare the area and the power consumption of the OTA of the second integrator. Moreover, we proposed a background calibration technique which removes the GVPN of the power efficient column-level SF-based reference buffers. The proposed calibration is best applied to high-speed, high-resolution imagers with column-level ISD ADCs.

ACNOLEDGEMENTS

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