9.8µm SPAD-based Analogue Single Photon Counting Pixel with Bias Controlled Sensitivity

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Abstract: **A scalable NMOS-only 11T SPAD-based analogue single photon counting pixel is presented. Implemented in advanced 130nm imaging low voltage CMOS, with no extra implants, a state of the art 9.8µm pitch is achieved. Novel pixel operation using a charge transfer amplifier (CTA) allows bias controlled sensitivity from 13.1mV/event to 150µV/event. Less than 2% PRNU is measured in the sensitivity range 5.5mV to 13.1mV per event with <0.01e⁻ input referred noise. A second mode operates the CTA as a switched current source enables the pixel to operate as a fast time-gated Quanta Image Sensor pixel.**
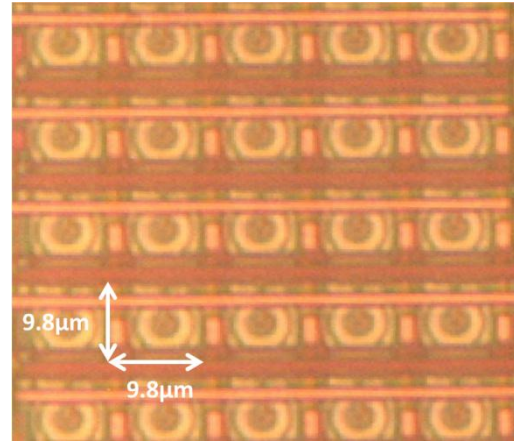
Fig.1 Photomicrograph of the SPC Test Array

I. INTRODUCTION

Single photon counting (SPC) image sensors have a number of applications such as time-of-flight (TOF) ranging and advanced microscopy [1][2][3]. CMOS single photon avalanche diode (SPAD) based image sensors offer the combined advantage of integration of electronics and high timing precision. In CMOS SPAD-based pixels, a trade-off exists between pixel pitch, fill factor and in-pixel functionality. Henderson et al. [4] have presented the smallest reported pitch of 5µm using minimal in-pixel circuitry. Higher fill factor is achieved by [1] and [5] by placing the timing or counting circuitry outside the array, yet this puts a limitation on signal routing and increases bus-sharing affecting scalability to mega-pixel arrays. By comparison, Walker et al. [6] implemented a high degree of functionality using an all-digital pixel with a 44.65µm pitch at the cost of 3.2% fill factor. A good compromise was reached by Pancheri et al. [3], who utilised an analogue SPC within 25µm pitch with 21% fill factor. However, in that work the current consumption of the NMOS-only inverter limits integration into a large array. The pixel proposed by Panina [7] has a high transistor count, and adding PMOS devices increases the pitch because of N-Well spacing rules. The NMOS-only SPC proposed by Chitnis [8] uses the SPAD 'on' time to control a current discharge with the disadvantage that the voltage step is quench voltage and dead-time dependent.

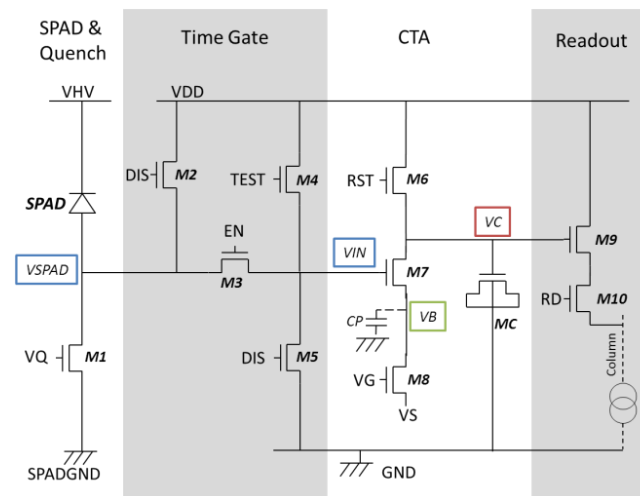In this paper, we present a NMOS-only, zero static bias current, 11T SPAD-based analogue SPC pixel in 130nm

Fig.2 Pixel Schematic

low voltage CMOS with no extra implants. We achieve a state of the art 9.8µm pixel pitch for a SPC SPAD pixel, which is scalable to large arrays. We demonstrate novel and versatile pixel operation utilising a charge transfer amplifier (CTA) to produce a variable voltage step, allowing voltage controllable sensitivity from 1.08V/event to 150µV/event, and hence electrically adjustable full well capacity from 1 to 1,000 events.

II. SPC PIXEL

A photomicrograph of the 3x3 SPC test array, with surrounding dummy pixels, is displayed in Fig.1. The SPAD is a modified P-Well to deep N-Well structure from [9] with a 2µm diameter anode and a reduced guard ring to facilitate the sub-10µm pitch. It has 99Hz
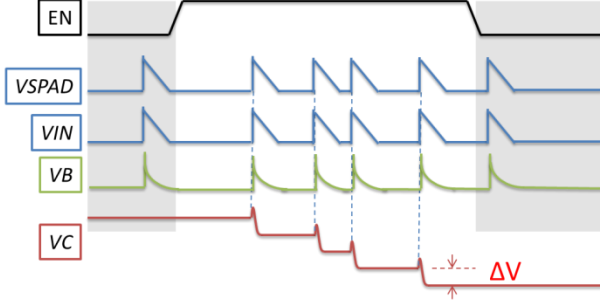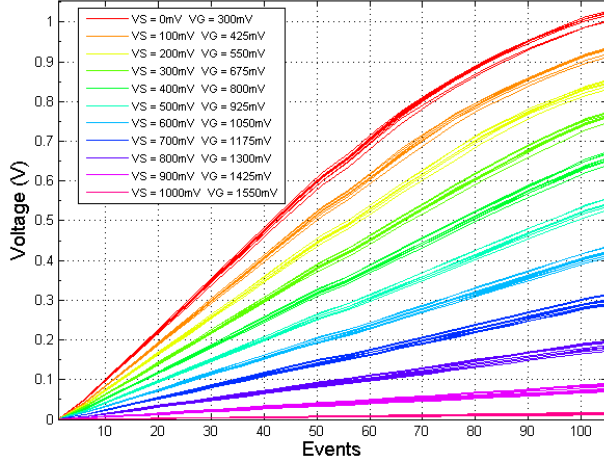
Fig.3. CTA Timing Illustration

Fig.4. Emulation of 9 Pixels in CTA Mode – 1 to 100 Events

median dark count rate (DCR). The pixel has a 3% fill factor with the single isolated SPAD and compact surrounding electronics. The schematic is shown in Fig. 2. It consists of four parts: SPAD and quench, time gate, CTA and standard APS-based readout. To realise SPC operation with controllable sensitivity the pixel is operated in two distinct modes. The first operates the pixel as a CTA: It functions by transferring charge from the capacitor MC (17fF) to the parasitic capacitance C_P (~0.1fF) at node V_B. This operation is achieved by biasing M8 in sub-threshold, with M8 acting as a high valued resistance. CTAs derive from low-power A/D converters [10]. Fig. 3 illustrates the CTA mode timing. The second mode operates the CTA as a switched current source (SCS), with M8 above threshold, enabling fast single photon detection.

In CTA mode, the magnitude of the voltage step 'ΔV' is determined by the capacitance ratio and the V_{GS} of the dynamic source follower M7 (formed by the input voltage V_{IN} and by V_B). The step size (ΔV) is therefore bias adjustable:

$$\Delta V = (\Delta V_{IN} - V_S - V_T) \cdot (C_P/C_{MC}) \qquad (1)$$

The 'V_S' bias allows the control of the step size and the 'V_G' bias is used to compensate for the body effect on the threshold voltage, which is estimated in the characterisation. The pixel response characteristic, in CTA mode, is emulated by using the M4 test transistor.

An example of an emulated graph is shown in Fig. 4. Both the emulation and SPAD mode use a high voltage, on the gates of M4 or M3 respectively, to reduce the relative contributions of their V_T variability. As shown in equation (1), the pixel sensitivity is dependent on the source bias voltage 'V_S' and this relationship is displayed in Fig.6. The first order equation (1) has been fitted to Fig.6 to confirm the CTA operation (ΔV_{IN} is assumed to be a constant value and an approximation from simulation is made for parameters V_T and (C_P/C_{MC})). The pixel response non-uniformity (PRNU) is proportional to the variability of each voltage step. Therefore operating with lower sensitivity, the step variability is a higher proportion of the step magnitude. The PRNU is expressed in equation (2) where V_P is the counter output peak voltage after CDS, N is the full well capacity, $\sigma_{\Delta V}$ is the std. deviation of the voltage step variability and σ_I represents the noise contribution from other sources independent of 'V_S' bias (e.g. read and ADC noise during readout). Equations (3.1) and (3.2) shows the std. deviation $\sigma_{\Delta V}$ under different inputs assuming the source follower gain is unity, where $(\sigma_{VSPAD})^2$ is the variance of the SPAD during avalanche and $(\sigma_{VT\_M7})^2$ is the variance of the V_T of the source follower M7.

$$\text{PRNU} = \sqrt{\left(\frac{\sigma_{\Delta V} \cdot N}{Vp}\right)^2 + (\sigma_I)^2}$$

$$\text{PRNU} = \sqrt{\left(\frac{\sigma_{\Delta V}}{\Delta V}\right)^2 + (\sigma_I)^2} \qquad (2)$$

With SPAD input:

$$\sigma_{\Delta V} = \left(\frac{C_P}{C_{MC}}\right) \cdot \sqrt{\left(\sigma_{VT\_M7}\right)^2 + (\sigma_{VSPAD})^2} \quad (3.1)$$

With emulation input:

$$\sigma_{\Delta V} = \left(\frac{C_P}{C_{MC}}\right) \cdot \sigma_{VT\_M7} \quad (3.2)$$

Equation (2) is fitted using the same parameters as Fig. 6 and plotted against measured PRNU values in Fig. 7.

III. RESULTS

The 3x3 array has an analogue column output connected to a 14b external ADC for characterisation. Correlated multiple sampling (CMS) is used to sample the analogue output, as shown in Fig. 5, with 4096 samples before and after integration to suppress reset noise. The ADC noise contribution is evaluated at 426µV RMS by tying the inputs together to a mid-rail bias. This ADC noise is dominant in our experimental setup, which masks the output source follower M9 noise contribution (RTS, 1/f and thermal) and the kT/C noise of the in-pixel capacitance C_{MC}.
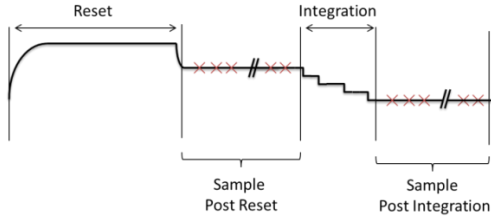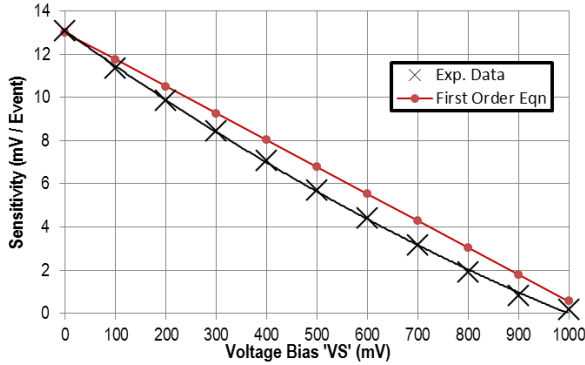
Fig.5. Correlated Multiple Sampling Timing Diagram
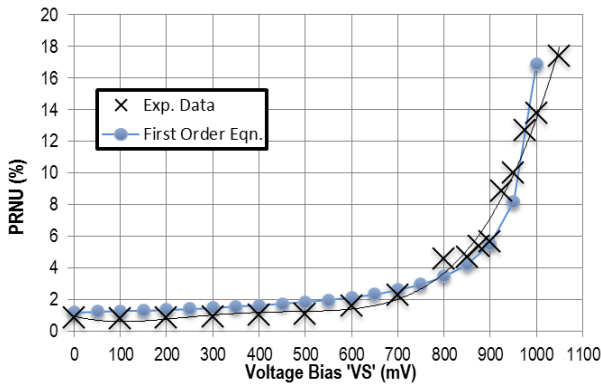

Fig.6. Pixel Sensitivity versus Voltage Bias 'V$_S$'

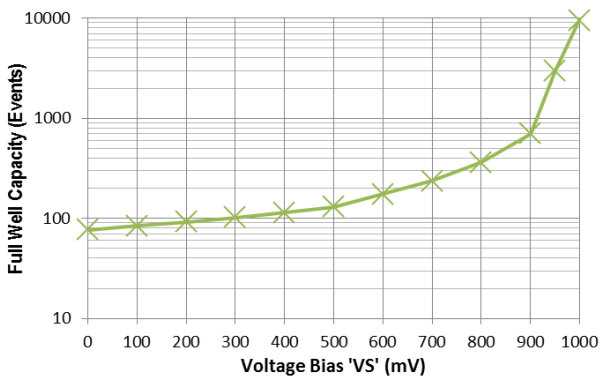Fig.7. Pixel Response Non-Uniformity versus Voltage Bias 'V$_S$'

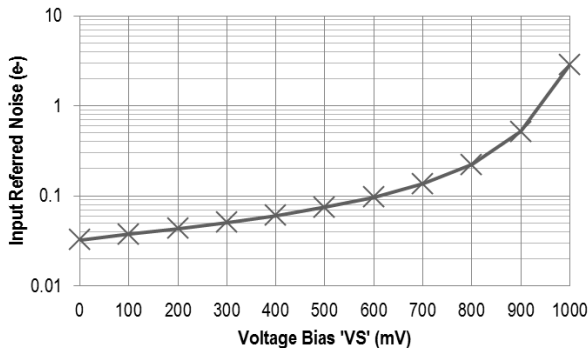Fig.8. Full Well Capacity versus Voltage Bias 'V$_S$'

Fig.9. Input Referred Noise versus Voltage Bias 'V$_S$'

The pixel sensitivity and full-well capacity were measured against a sweep of 'V$_S$' bias in CTA mode, and the PRNU and input referred noise were calculated. These results are plotted in figures 6 to 9. PRNU less than 2% is obtained in the range of 'V$_S$' bias 0mV to 600mV with corresponding sensitivity range 5.5mV to 13.1mV per event and input referred noise 0.03e$^-$ to 0.1e$^-$. Greater dynamic range and lower sensitivity are obtainable at the cost of high PRNU and higher noise. The pixel variability rapidly degrades to 17.4% PRNU as 'V$_S$' bias is swept to 1V with 150 µV per event sensitivity and 2.8e$^-$ input referred noise.

The SCS mode measurement results are included in figures 10 to 13. The sensitivity is measured with steps of 108mV/event to the full swing of 1.08V/event with corresponding full well of 10 to 1 events. The input referred noise across the same range varies from 0.004e$^-$ to 0.0004e$^-$. High variability is evident in SCS mode, precluding accurate counting operation but instead offering coarse detection of zero, one or few photons. A pixel array implementation utilising high-speed readout would serve as a time-gated Quanta Image Sensor, proposed by Fossum in [11].

The pixels were tested under light with the SPADs enabled in CTA mode. Fig.14 demonstrates the discretised Poisson-distributed output voltage histogram from all pixels at varying bias under constant light, clearly illustrating the voltage step controllability.

CONCLUSION

An 11T, NMOS-only SPAD-based SPC pixel is implemented in low voltage 130nm imaging CMOS with no extra implants. Charge transfer amplifier operation allows bias controlled sensitivity from 13.1mV/event to 150µV/event. PRNU < 2% is measured operating in the 'V$_S$' bias range from 0 to 600mV with sensitivities from 13.1mV to 5.5mV per photon and 0.03e$^-$ to 0.1e$^-$ input referred noise respectively. Higher 'V$_S$' bias increases the pixel dynamic range and decreases sensitivity at the cost of high PRNU. A second switched current source mode facilitates high-speed single photon detection. This pixel is scalable to large arrays offering high-resolution single photon imaging in the near future for TOF and advanced microscopy applications.

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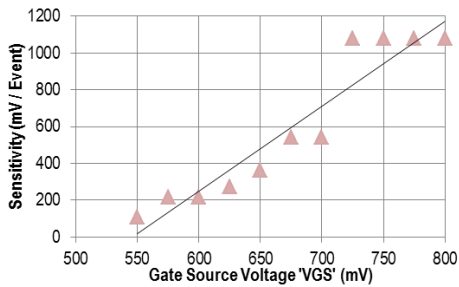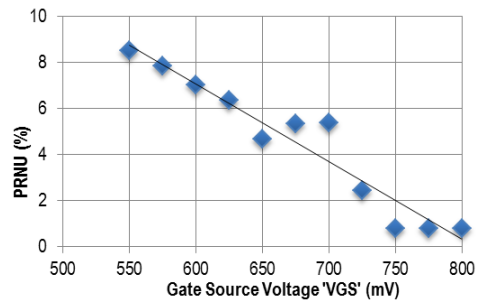
Fig. 10. SCS Mode Pixel Sensitivity versus M8 V_{GS}
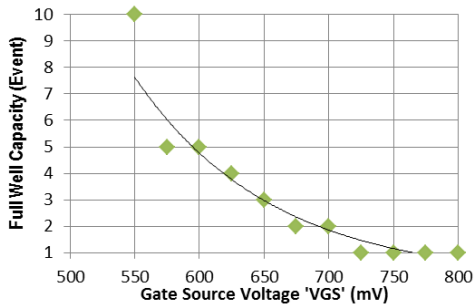

Fig. 11. SCS Mode PRNU versus M8 V_{GS}

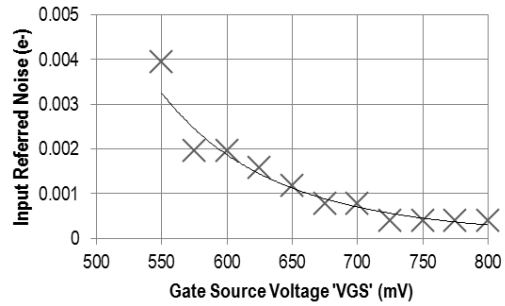Fig.12. SCS Mode Full Well Capacity versus M8 V_{GS}

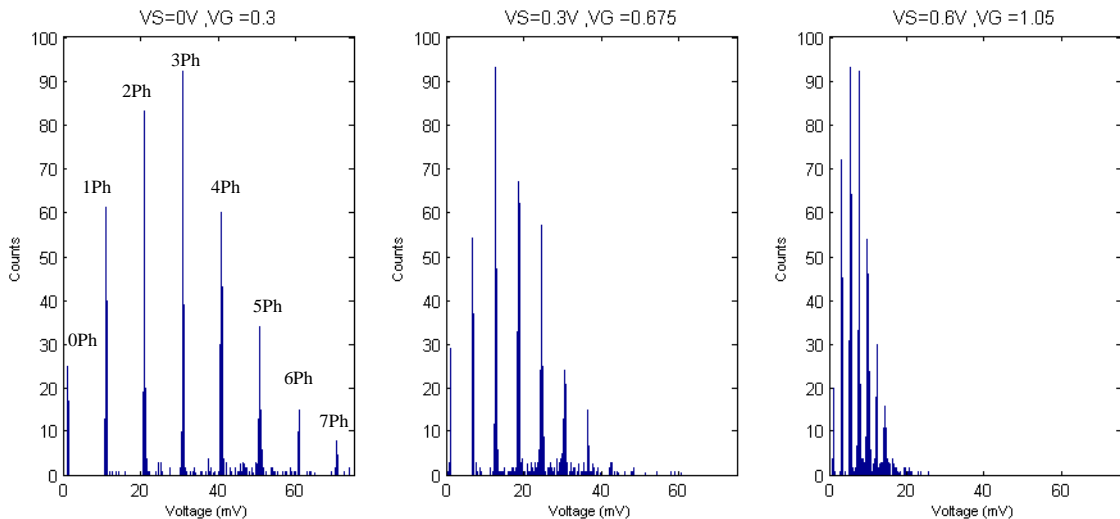Fig. 13. SCS Mode Input Referred Noise versus M8 V_{GS}

Fig.14. Output Voltage Histograms For All Pixels at Varying Voltage Bias Under Constant Light