A FSI CMOS Image Sensor with 200-1000 nm Spectral Response and High Robustness to Ultraviolet Light Exposure

Rihito Kuroda, Shun Kawada, Satoshi Nasuno, Taiki Nakazawa, Yasumasa Koda, Katsuhiko Hanzawa and Shigetoshi Sugawa
Graduate School of Engineering, Tohoku University
6-6-11-811, Aza-Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, Japan 980-8579
TEL: +81-22-795-4833, FAX: +81-22-795-4834, Email address: kuroda@fff.niche.tohoku.ac.jp

ABSTRACT

A 5.6 μm pixel pitch FSI-CMOS image sensor using highly ultraviolet light (UV-light) sensitive and highly robust photodiode (PD) technology was fabricated and evaluated. In-pixel buried pinned-PD having a the p^+ layer with a steep dopant profile uniformly formed on a flattened Si surface was integrated for improvements of sensitivity and robustness to UV-light. The fabricated chip exhibited a spectral response to the wide light waveband of 200 to 1000 nm, and sensitivity degradation did not occur after the strong UV-light exposure stress.

INTRODUCTION

Image sensors and photodiode arrays with a wide spectral response, including ultraviolet light (UV-light) waveband of 200-320 nm, is strongly required in the fields of various spectrophotometric analysis, biological phenomena analysis, environmental assessment, space vision, etc. For the image sensor development, an improvement of UV-light sensitivity and an improvement of sensitivity robustness to UV-light exposure have been challenges [1-2]. Especially, due to the short penetration depth of UV-light in Si, the atomic scale control of the dopant profile of the light incident side Si surface region to form a photo-generated carrier drift layer is required [3]. UV-light sensitive BSI-CCD, BSI-CMOS with additional backside surface treatment process, and detector-on-Si type CMOS imagers have been reported [3-5]. In the last IISW in 2011, we demonstrated a highly UV-light sensitive and highly robust Si photodiode (PD) technology using an atomically flattened (100) oriented Si surface [6]. In the developed photodiodes, a thin surface photo-generated carrier drift layer with steep dopant profile was uniformly formed so as to improve the sensitivity and sensitivity robustness to UV-light. In this work, by integrating the developed photodiode technology into a CMOS image sensor fabrication process, we demonstrate a FSI-CMOS image sensor with a wide spectral response from 200 to 1000 nm and a high robustness to UV-light exposure.

PHOTODIODE TECHNOLOGY

Figure 1 shows the schematic illustration of the cross sectional view of in-pixel buried pinned-PD, transfer gate and floating diffusion (FD) and Fig. 2 shows the illustration of dopant profile of top p^+n junction and key features to achieve a high sensitivity and a high robustness to UV-light.

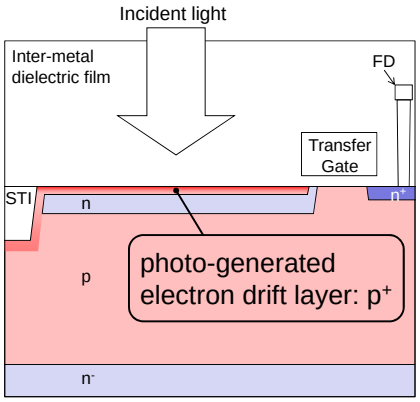


Fig. 1. Schematic illustration of the cross sectional view of photodiode, transfer gate and floating diffusion. The photo-generated electron drift layer was formed at the top surface of the PD.

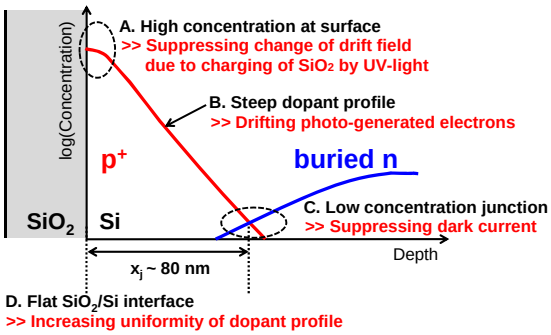


Fig. 2. Illustration of the dopant profile of top p^+n junction and key features to achieve a high sensitivity and a high robustness to UV-light.

Followings are the summary of the key features and technologies to obtain a high sensitivity and a high robustness to UV-light.

A. Sufficiently high dopant concentration at the top few nanometer Si surface to form a thin neutral region. Here, both fixed charges and interface states increase due to a strong UV-light exposure, and this induces a sensitivity change and a dark current increase to photodiode [7]. The purpose of "A" is to suppress the change of drift field due to a charging (fixed charge generation) of SiO_2 film by injection of high energy photo-generated carriers as well as, to deactivate interface states.

B. Steep dopant profile of surface p^+ layer to form an electric field to drift photo-generated electrons to buried n layer. The electric field of this photo-generated carrier drift layer is induced by space charges of depletion layer and gradient of hole concentration of top neutral region.

C. Low concentration junction between surface p^+ layer and buried n layer. The purpose of this is to reduce the electric field at the pn junction to suppress dark current. In addition, the junction depth (x_j) and dopant concentration at the junction is designed so that the depletion layer does not reach the incident light side Si surface when the buried n layer is fully depleted. For the fabricated CMOS image sensor, the x_j was 80 nm.

D. Atomic scale flatness of SiO_2/Si interface. It is required so as to uniformly form the above mentioned thin and steep dopant profile uniformly. Here, the roughness of the Si or SiO_2/Si interface induces a variation of dopant profile during the low energy ion implantation for p^+ layer formation.

In addition to above mentioned key features: A-D, following process technologies are also important; A high quality SiO_2 film and Si/SiO_2 interface formation process to reduce the increases of fixed charge of SiO_2 film (due to trapping of injected carriers) and interface state during UV-light exposure, a low energy ion implantation process for steep p^+ profile formation, and a low thermal budget annealing process for activation of the steep-profile dopant and defect recovery.

IMAGER DESIGN AND CHIP FABRICATION

A 5.6 μm pixel pitch FSI-CMOS image sensor with buried pinned-PD having surface photo-generated electron drift layer explained in the previous section was fabricated. Figure 3 shows the pixel circuit schematic. The lateral overflow integration capacitor (LOFIC) pixel architecture was employed for a high conversion gain (CG) and high full well capacity (FWC) performance [8-9]. A wide dynamic range and high sensitivity linear response imaging is achieved with a single exposure by CMOS image sensor with LOFIC [8-9]. The image sensor chip was fabricated using a 0.18 μm 1P3M CMOS process technology. For the formation of thin and steep p^+ layer, process conditions related to the Si surface flatness, ion implantation for PD and activation anneal were tuned to integrate the highly UV-light sensitive and highly robust PD. Figure 4 and table 1 show the micrograph and the design specification of the developed chip, respectively. The developed chip does not have microlens.

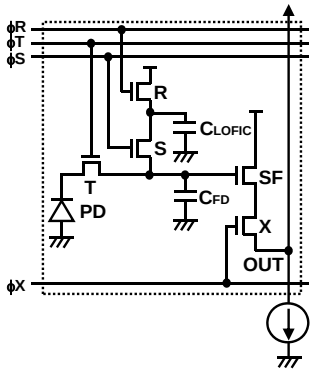


Fig. 3. Pixel circuit schematic of the fabricated chip.

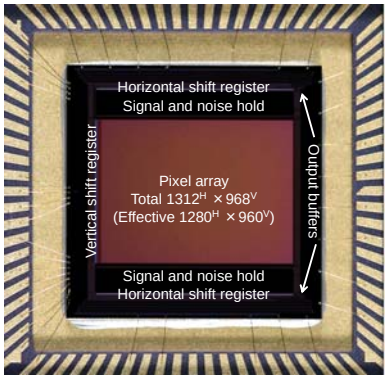


Fig. 4. Chip micrograph.

Table 1. Design specifications of the fabricated chip.

Process technology		0.18 μm 1P3M CMOS with pinned-PD
Supply voltage		3.3 V
Die size		$9.5^H \times 9.5^V$ mm^2
Pixel size		$5.6^H \times 5.6^V$ μm^2
Number of pixels	Total	$1312^H \times 968^V$
	Effective	$1280^H \times 960^V$
Fill factor		26 %

EVALUATION RESULTS

From the measured photoelectric conversion characteristic, the CG and FWC were 109 V/e^- and 1.2×10^5 e^-, respectively. Due to the small FD capacitance and a large LOFIC capacitance, high CG and FWC were obtained simultaneously. The PD dark current at 60 ˚C was 8.3 e^-/sec-μm^2, and no increase of dark current was detected due to the UV-light exposure stress explained below.

Figures 5 and 6 show the picture of the UV-light exposure stress system and the spectral distribution of the UV-light source employed for the evaluation of the sensitivity and dark current stabilities of the fabricated chip. The super high pressure mercury discharge lamp was employed for this evaluation. The typical UV-light intensities are 2.0, 4.4, 8.8 and 17.6 mW/cm^2 for the wavelength of 254, 303, 313 and 365 nm, respectively. The UV-light exposure stress was applied for 1000 min. The total amount of the light exposure after 1000 min was 1.2x10^2, 2.6x10^2, 5.3x10^2 and 1.1x10^3 J/cm^2 for the wavelength of 254, 303, 313 and 365 nm, respectively. Spectral response and dark current were measured before and after the UV-light exposure.

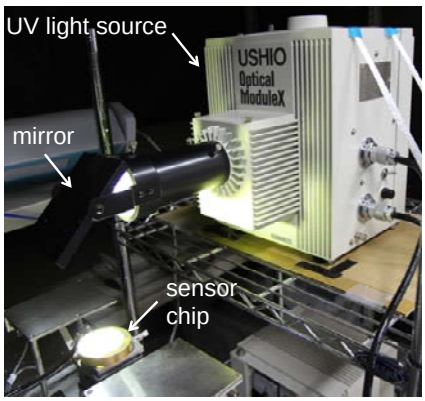


Fig. 5. Picture of UV-light exposure stress system.

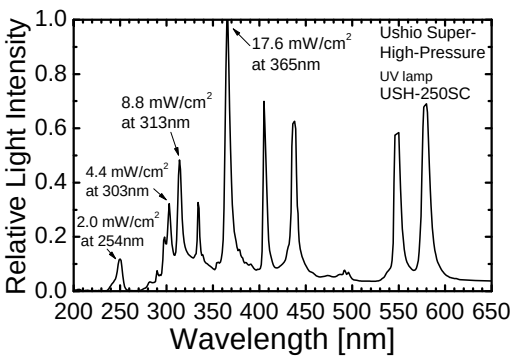


Fig. 6. Spectral distribution of the UV-light source used for the UV-light exposure stress.

Figure 7 shows the spectral response of the fabricated CMOS image sensor measured before and after the UV-light exposure stress for 1000 min. For both cases, the high photosensitivity was obtained for a wide light waveband of 200 to 1000 nm. In addition, it was confirmed that almost no degradation of spectral response occurred for the developed CMOS image sensor.

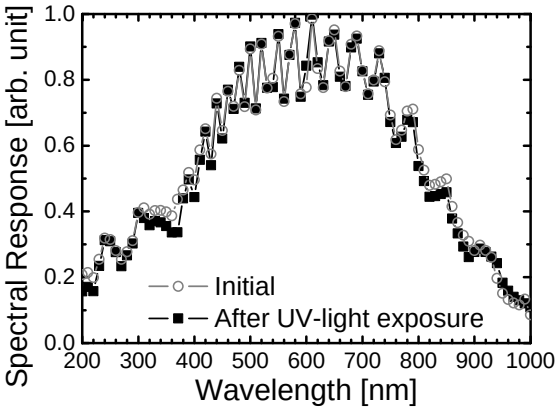
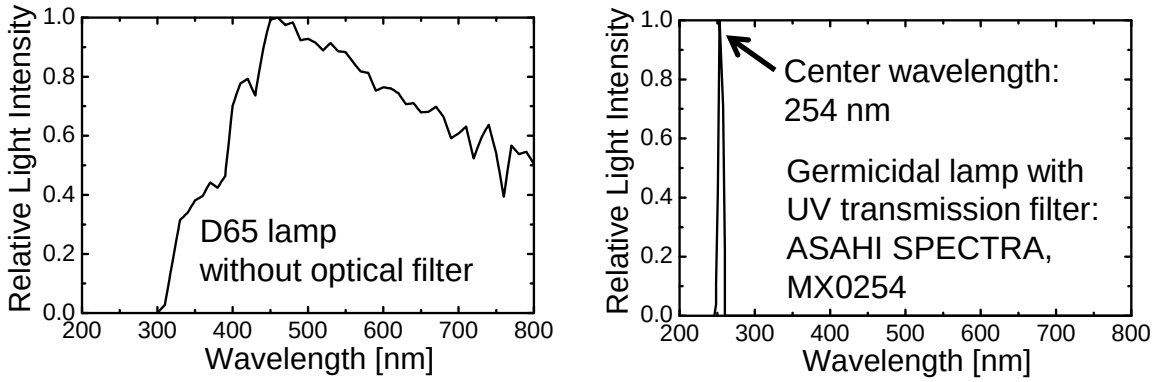


Fig. 7. Spectral response of the fabricated CMOS image sensor chip measured before and after the UV-light exposure stress.

Figure 8 shows the spectral distribution of the irradiated light during the sample image capturing, (a) D65 lamp without optical filters having a broad distribution from 300 to at least 800 nm, and (b) germicidal lamp with an UV transmission filter having a narrow distribution around 254 nm. During the sample image capturing, an UV-light transmission lens: PENTAX B2528UV was employed. Figure 9 shows the captured sample images of a stuffed doll, fruit and other objects, an incandescent lamp and a white paper with a picture drawn by a sun block cream containing UV-light absorbent. The picture on the white paper is clearly observed when the germicidal lamp was irradiated.

CONCLUSION

A 5.6 μm pixel pitch FSI CMOS image sensor with the buried pinned-PD having the thin and steep p^+ layer of photo-generated electron drift layer was fabricated and evaluated. The fabricated chip exhibited a spectral response to the wide light waveband of 200 to 1000 nm, and sensitivity degradation did not occur after the strong UV-light exposure stress. The developed in-pixel photodiode formation technology is applicable to various types of Si image sensors and array sensors for wide waveband light detection and imaging.



(a) (b)

Fig. 8. Spectral distribution of the irradiated light for image sensor chip during the sample image capturing. (a) D65 lamp without optical filters and (b) germicidal lamp with an UV-light transmission filter: ASAHI SPECTRA, MX0254.

(a) (b)

Fig. 9. Sample images of a stuffed doll, fruit and other objects, an incandescent lamp and a white paper with a picture drawn by a sun block cream containing UV-light absorbent. (a) the image taken with a D65 lamp without optical filters and (b) the image taken with a germicidal lamp having the center wavelength of 254 nm and an UV-light transmission filter. Both images were taken with an UV-light transmission lens, PENTAX B2528UV.

ACKNOWLEDGEMENT

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