A direct-detection X-ray CMOS image sensor with 500 μm thick high resistivity silicon

T. Hatsui[1,2,*], M. Omodani[2], T. Kudo[1], K. Kobayashi[1,2], T. Imamura[3], T. Ohmoto[3], A. Iwata[3], S. Ono[1], Y. Kirihara[1], T. Kameshima[2], H. Kasai[4], N. Miura[4], N. Kuriyama[4], M. Okihara[5], Y. Nagatomo[5], M. Nagasaki[6], T. Watanabe[7], Makina Yabashi[1,2]

[1]RIKEN SPring-8 Center, [2]JASRI, [3]A-R-Tec Corp, [4]LAPIS Semiconductor Miyagi Co., Ltd., [5]LAPIS Semiconductor Co., Ltd., [6]ARKUS Inc, [7]University of Hyogo

[1]RIKEN, SPring-8 Center, 1-1-1 Kouto, Sayo-cho, Sayo-gun, Hyogo 679-5148, Japan

Abstract

This paper reports recent results of a direct-detection X-ray CMOS image sensor for X-ray Free-Electron Laser (XFEL) experiments. The sensor incorporates the in-pixel dual gain circuitry by using Fully Depleted-Silicon-On-Insulator (FD-SOI) CMOS transistors located on top of the buried oxide (BOX) layer. Beneath of the BOX layer, high resistivity handle wafer made from floating zone method was formed as p-n junction diode to detect X-rays. Between the handle wafer and the FD-SOI CMOS, via through BOX layer is formed to transfer the charge. This paper describes the production method and sensor architecture of the sensor. In addition to the scientific demands of XFEL experiments, a general X-ray imaging application by using this sensor architecture is also presented.

1. Introduction

Recent advances in X-ray Free-Electron Laser (XFEL) technologies have enabled production of full spatial coherence, ultra-short pulse duration, and high brilliance laser in X-ray frequency domain[1, 2]. A wide range of applications are anticipated with the novel light source characteristics, and some of them have already proved its capability by recent works at the LCLS and SACLA, which are operational form 2009, and 2012, respectively. In many of XFEL applications at these facilities, novel X-ray Imaging detector is required. Hybrid sensor, CS-PAD[3], custom radiation hard CCDs such as pnCCD[4] or Multi-port CCDs are deployed. These have common functionalities, such as single photon detection. XFEL Science is, however, demanding more advanced imaging sensor, especially, larger imaging area, and higher peak signal.

In this paper, recent results of the development of a direct-detection X-ray CMOS image sensor, SOPHIAS (Silicon-On-Insulator Photon Imaging Array Sensor) is presented. The target application of this sensor is the coherent X-ray Diffraction imaging experiments. We set the minimum performance requirement as (1) single X-ray photon sensitivity for 5.5-7 keV range, (2) 60 frame/sec, (3) less than 6 pixel dead area, and (4) high peak signal of 7 Me-/pixel with 30 μm square pixel.

2. Process Development

We have developed a 0.2 μm fully-depleted Silicon-On-Insulator (FD-SOI) technology for X-ray pixel detector[5, 6]. This technology enables separate optimization of the CMOS circuitry on Silicon-On-Insulator layer and p-n junction diode. In the study, floating zone wafer is used as high resistivity silicon source for the p-n junction diode. In the direct-detection X-ray CMOS sensor, depletion as thick as 150 μm is required in order to achieve the quantum efficiency over 95 % in the target 5.5-7 keV photon energy range. Furthermore, the back-illumination geometry with thick *p-n* junction diode attenuates incoming X-ray significantly so that the radiation against the CMOS transistors can be minimized. The attenuation for 5.5-7 keV X-ray photon with 500 μm silicon ranges from 6.4×10^{-10} to 2.5×10^{-5}. FD-SOI process has radiation hardness against total ionizing doe up to around 150 krad(Si). Together with the 500 μm handle wafer attenuation, effective 6 Grad(Si) radiation hardness can be achieved. Main characteristics of the process used for SOPHIAS sensor production is tabulated in Table 1.

The detector sensitive area will be formed by an array to be up to 40 sensors with an area of 260 mm x 260 mm with 76 Mpixels. In such a tiled sensor system, sensor size should be large enough that the readout electronics of each sensor can fit to the footprint of the sensor. In the present study, large sensor size is achieved by introducing a stitching lithography technique for substrate implants, vias through BOX, and 1st metal layer. The floor plan is shown in Fig. 1. These layers connect the guard ring block, which isolate CMOS blocks from the high voltage applied to the back. The other blocks in central three shots are not stitched and operate independently. In between these shots, spacing matching one column width (30 μm) is placed. SEM image of the stitched region is shown in Fig. 2. The signals in this region without pixels are detected by the adjacent pixels. The missing data is obtained by averaging the neighboring column data similar to the other thick sensor detector[7]. The row registers, which are frequently placed at the side of pixel area, is moved to the bottom of the sensor so that the stitching of pixel region is not mandatory.

* Corresponding author, *hatsui@spring8.or.jp* phone +81-791-58-0802

All the other periphery circuits are also placed at the bottom of the sensor so that the SOPHIAS sensor can be 4-side butted with a stepped geometry. The fabricated wafer is shown in Fig. 3.

Backside of the wafer is processed after the CMOS fabrication by using CMP, wet etching, implant, laser annealing, and aluminum deposition with thickness of 200 nm. The implant condition is optimized for X-ray so that the insensitive layer thickness is about 0.3 um. The charge collection efficiency simulated by device simulation code Silvaco Atlas is shown in Fig. 4. The insensitive layer together with aluminum optical blocking filter gives overall transmittance more than 98 % for 5.5-7 keV X-rays.

3. Sensor Architecture and Performance

In the case of X-ray direct detection by silicon, about 1900 electron-hole pairs are generated from single X-ray photon at 7 keV since silicon have an effective ionization energy of 3.65 eV[8]. In order to achieve dynamic range of 60, single pixel should have peak signal of 3600 photons, equivalent to 7 Me-. In order to detect single photon, we set the noise target to 150 e-rms by considering a threshold analysis scheme.

The high peak signal of 7 Me- (1.12 pC) demands large capacitance within the pixel. By using the MIM capacitance of the current process, the area becomes about 750 μm^2 with signal swing of 1 V, which is close to the pixel size of 30 μm square. In order to achieve this large peak signal detection while keeping single photon sensitivity, a multi-via concept has been developed, where the signal charge is divided before the amplification step. In this scheme, a small fraction of the signal charge is transferred to the lower gain amplifier, while the large fraction is delivered to high gain amplifier (Fig. 5). Implemented schematic diagram is described in Fig. 1. The pixel circuit has no transmission gate. The input capacitances including stray capacitance are 16 and 240 fF for high and low gain channels, respectively. With the multi-via concept, designed gain difference is to be 48 whereas the input node capacitance of the low gain is only 15 times larger. Each pixel output line is connected to column buffers, and then to 24 parallel output stages, which operates at the pixel readout rate of 25 MHz to operate at 60 frame/sec.

The sensor performance was evaluated by a sensor evaluation test bench. Readout noise was estimated to be around 600 e-rms for high gain channel, which was dominated by the test bench system. The noise performance is inferior to the target performance, however, the sensor is still detecting the single photon level because single X-ray photon generates 1500-1900 e- in 5.5-7 keV.

In order to assess the full depletion condition, line spread function as a function of bias voltage to the backside was evaluated by using an edge method (Fig. 6). A Cu Kα X-ray source at 40 kV, 0.3 mA was used. At 120 V, the line spread function becomes less than 2 pixel, and converges to about 1 pixel at higher bias voltage. This implies that the 500 μm thick p-n junction diode is fully depleted at 120 V, equivalent to the resistivity of 7 kohm·cm.

Further optimization will be carried out for the SACLA user operation, especially, the noise minimization to achieve more accurate detection of single X-ray photon, the flicker noise reduction, and suppression of the background drift.

To demonstrate the capability in general X-ray analysis, projection image of a dried sardine was taken with an bias voltage of 200 V. The obtained image is shown in Fig. 7. Clear fine structure was observed within 1 sec exposure with a conventional laboratory X-ray source. The image indicates that this sensor is of value for general X-ray imaging and analysis as well.

4. Conclusion

The sensor for XFEL experiments, SOPHIAS has been developed. The sensor fabricated from SOI wafer enables monolithic CMOS sensor with fully depleted p-n junction diode as thick as 500 μm. By using a stitching lithography, large sensor of 64.77(v.) x 26.73 (h.) mm^2 was successfully manufactured. The sensor size together with the layout with all the periphery confined to the bottom region provide 4-side buttable geometry.

In contrast to the indirect X-ray detectors, where optical photons converted from X-rays emitted without preferred direction, the developed sensor with thick depleted p-n junction diode provides internal potential to sweep the signal charge toward the CMOS pixel circuitry. This mechanism gives high spatial resolution while keeping quantum efficiency. The advantage of this sensor has been demonstrated for conventional projection X-ray imaging.

5. Acknowledgements

We wish to dedicate this paper to the memory of Dr. Mitsuru Nagasono, who passed away during this study.

Table 1. Parameters of the Fabrication Process for SOPHIAS

Process	0.2 μm Low-leakage Fully-Depleted SOI CMOS, 1 poly, 5 Metal layers, MIM cap. on 3rd metal layer, DMOS option, Core (I/O) Voltage = 1.8 (3.3)V
Transistors	Normal and low-Vt for both core and I/O transistors, Transistor layout options: body-floating, source-tie and body-tie *Only the IO transistors are used with voltage = 2.5 V for SOPHIAS design.*
SOI wafers	Diameter: 200 mm Top Si: CZ 10 ohm·cm, p-type 40 nm thick Buried oxide: 200 nm thick Handle wafer: floating zone, over 2 kohm·cm, n-type
Backside process	Thinned to 500 um by CMP, wet etching, implantation, laser annealing, and aluminum deposition.

Table 2. Specifications of the image sensor, SOPHIAS

Chip Size	65.6 (v.) x 30.0 (h.)mm^2
Sensitive Layer	Floating zone handle wafer with depletion depth of 500 μm
Pixel Format	891 (v.) x 2159 (h.)
Imaging Area	64.77(v.) x 26.73 (h.)mm^2
Power Supply	2.5 (digital), 2.5 V(analog), 200 V (bias)
Pixel Size	30 μm
Shutter	Global Shutter
Frame Rate	60 fps
Gain	In-pixel Dual Gain
Noise	150 e-rms
Peak Signal	7 Me-
Output interface	12 analog readout port
Output Port	Single output port consists of high and low gain with quasi-differential outputs (total 4 analog outputs)

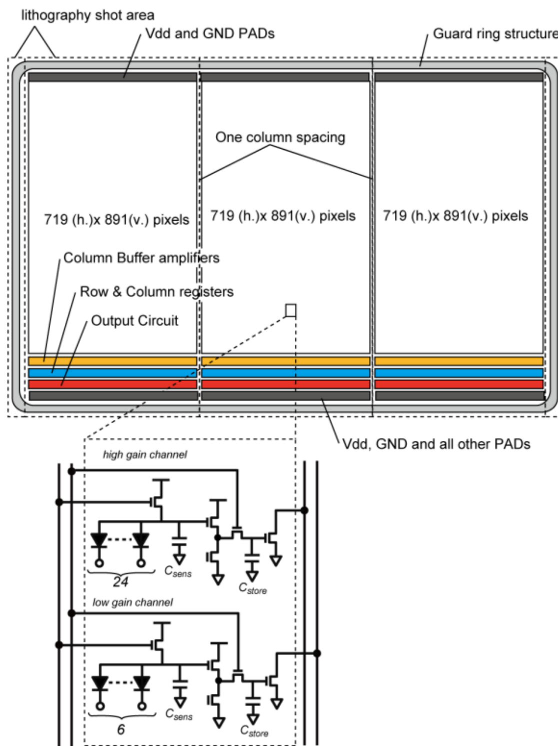

Fig. 1 Floor plan and pixel schematic diagram.

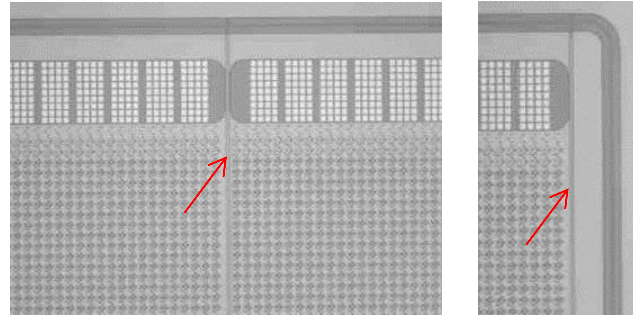

Fig. 2 SEM image of SOPHIAS around stitched area between pixel shots (left) and between pixel and guard ring shots (right). Stitched reagion is indicated by arrows.

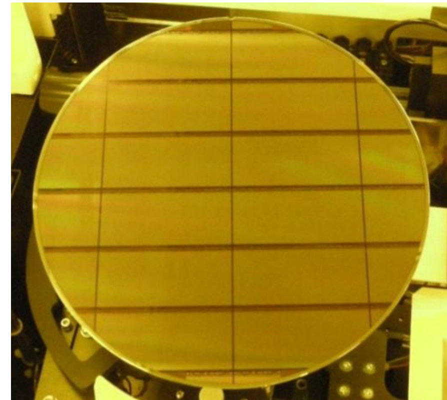

Fig. 3 A photograph of the sensors fabricated on 8 inch wafer.

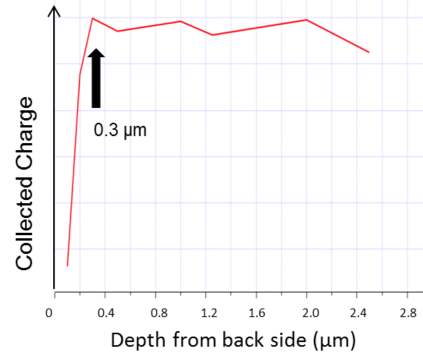

Fig. 4 Device simulation results on charge collected charge with the optimized backside doping condition as a function of the signal charge deposition distance from the backside of the sensor. Effective thickness of the insensitive layer is simulated to be around 0.3 μm.

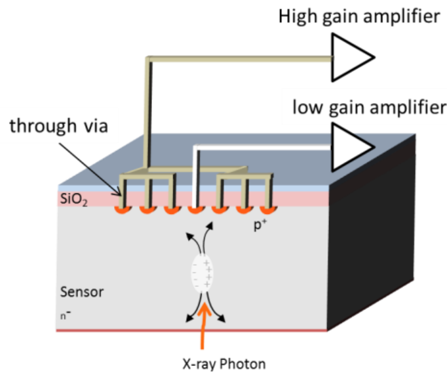

Fig. 5 Schematic Structure of the pixel. X-ray is illµminated from the backside and generates electron hole pairs. Holes are collected to the amplifier through the P+ implants of the handle wafer.

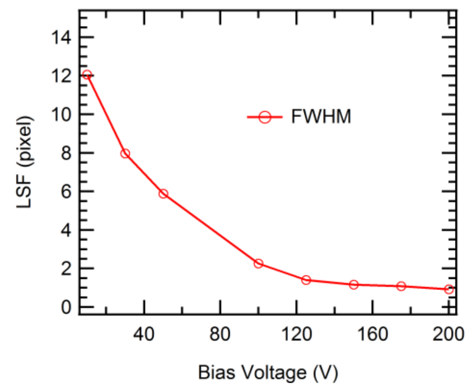

Fig. 6 Full-width half maximum of the line spread function measured by an edge method by using Cu Ka X-ray source with 40 kV, 0.3 mA.

Fig. 7 An X-ray projection image of a dried sardine taken by a conventional micro-focus X-ray source with a Cu target at the operation of 40 kV 0.8 mA. Background and flat field calibration was carried out. Exposure time of 1 sec, and a projection magnification of 2 were used. Inset shows the optical image of the sample.

Reference

1. P. Emma, et al., Nature Photonics 4 (9), 641-647 (2010).
2. T. Ishikawa, et al., Nature Photonics 6 (8), 540-544 (2012).
3. S. Herrmann, et al., Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment (0).
4. L. Struder, et al., Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment 614 (3), 483-496 (2010).
5. Y. Arai, et al., Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment 636, S31-S36 (2011).
6. Y. Arai, et al., Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment 623 (1), 186-188 (2010).
7. E. F. Eikenberry, et al., Nuclear Instruments & Methods in Physics Research Section a-Accelerators Spectrometers Detectors and Associated Equipment 501 (1), 260-266 (2003).
8. H. Spieler, Semiconductor detector systems. (Oxford University Press, Oxford ; New York, 2005).