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A 33 Mpixel, 120 fps CMOS Image Sensor for UDTV Application with Two-stage Column-Parallel Cyclic ADCs

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***Abstract*—A 33-megapixel, 120-frames/s (fps) CMOS image sensor (CIS) has been designed and developed for ultrahigh definition television (UDTV) applications. The CIS uses two-stage column-parallel cyclic analog-to-digital converters (ADCs) with 12-bit resolution. The ADC operation is pipelined in parallel and effectively reduces the conversion time. The ADC architecture also effectively lowers the power consumption by exploiting the amplifier function of the cyclic ADC. SPICE simulations achieved the conversion time shorter than 1.92 µs and total power consumption of the CIS approximately 2.5 W. The prototype image sensor with 2.8 µm × 2.8 µm pixel pitch, 7808 × 4336 pixels is developed using a 0.18-µm 1-poly 4-metal CIS process and driven at 120 fps.**

I. INTRODUCTION

In recent years, the demand for high-reality video systems has been increasing. Thus, NHK has been researching and developing ultra-high definition television as a next generation television broadcasting system called "Super Hi-Vision" (SHV). This system aims to improve the viewing experience by conveying the "sense of being there" and "sensation of realness" through wider and higher resolution pictures.

The full-spec parameter values for SHV video signal are 7680-pixel × 4320-line and 120 fps. The total pixel data output rate of the full-spec SHV image sensors will be 47 Gbit/s or greater. So far, several image sensors has been developed for UDTV or digital cinema applications [1-4], but they still do not yet fulfill the SHV specifications.

To meet the demand, we developed a 33-megapixel, 120-fps CMOS image sensor using high-speed, low-power two-stage column-parallel cyclic 12-bit ADCs. The column-parallel cyclic ADC has a short A/D conversion time and is suitable for high-speed image sensors [5]. To come up this advanced technology to fulfill SHV specifications, we divided the cyclic ADC to two stages. The pipelined and parallel operation of the 1st stage cyclic ADC and the 2nd stage cyclic ADC effectively reduced the conversion time and achieved 12-bit A/D conversion within the required horizontal scanning time period for 33 megapixels at 120 fps. Furthermore, this two-stage ADC structure also helped to reduce the power consumption of the ADC. We designed the 2nd stage cyclic ADC with very low power consumption, because the input signal of the 2nd stage cyclic ADC was amplified by the amplifier in the 1st stage cyclic ADC, and this amplified input signal significantly reduced the demand for noise and precision of the 2nd stage cyclic ADC circuit. Our SPICE simulation showed that the power consumption and the processing speed of the proposed ADC reached enough for our application. We also designed and fabricated the prototype image sensor with 2.8 µm × 2.8 µm pixel pitch, 7808 × 4336 pixels, and signal circuits using 0.18µm 1-poly 4-metal CIS process.

In this paper, we will describe the sensor architecture and overall operation in Section II, the detailed design and operation of the two-stage cyclic ADC in Section III, and the implementation and experimental results of the image sensor in Section IV.

II. SENSOR ARCHITECTURE

Fig. 1 shows the block diagram of the sensor. The pixel size of the sensor was 2.8 µm × 2.8 µm and the pixel array consists of 7808 × 4336 total pixels. On the top and bottom sides of the pixel array, there are correlated double sampling (CDS) circuits, two-stage column-parallel cyclic ADCs, latches, horizontal scanners, current mode

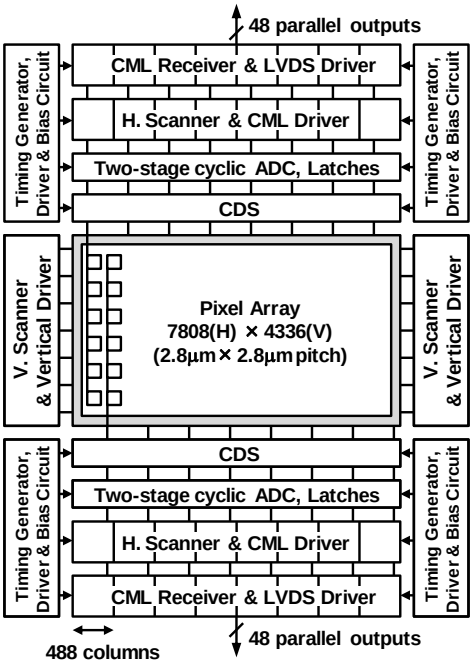

Fig. 1. Block diagram of 33Mpixel CMOS image sensor.

logic (CML) circuits, low-voltage differential signaling (LVDS) drivers, and on the left and the right sides, there are timing generators, drivers, and bias circuits. A 2.5-transister two-shared pixel architecture with pinned-photodiode is used for the pixels. The layout pitch of the column parallel circuits is 5.6 µm. Fig. 2 shows the operation sequence for the row cycles: analog CDS, 1st stage cyclic ADC, 2nd stage cyclic ADC, and horizontal readout. The CML, which enables low-voltage differential signal transfer, was used for horizontal data scanning during the A/D conversion. The horizontal scanners are divided into 16 parallel blocks to decrease the scanning speed, and each block scans 488 columns. The sensor has 96 parallel LVDS output ports on the upper and lower side of the sensor. The vertical scanners and drivers are placed on both the left and the right sides of the sensor. This prototype image sensor has also a region-of-interest (ROI) function. By using the function, this image sensor will also be able to be used as a 16-megapixel (7808-pixels × 2168-lines), 240-fps image sensor.

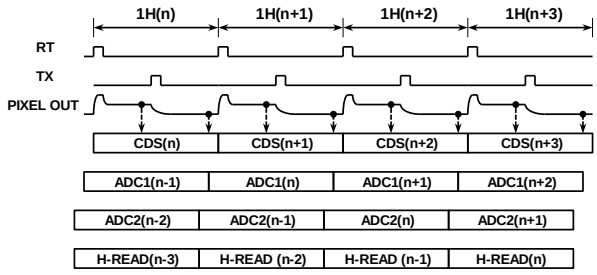

Fig. 2. Pipeline operation sequence for row cycles.

III. TWO-STAGE COLUMN-PARALLEL CYCLIC ADC

A. ADC Design

Fig. 3 shows a simplified schematic diagram of the two-stage cyclic ADC. The single-ended cyclic ADC with internal reference and return-to-zero (RTZ) digital signal feedback techniques [5] is used in each stage of the ADC. Each cyclic ADC generates three-state redundant binary (RB) codes expressed with two decision levels (2-bit) for each cycle to relax the comparator's precision demand [6]. Each cyclic ADC consists of a single-ended amplifier, capacitors (C_1 and C_2 for 1st ADC, C_3 and C_4 for 2nd ADC), sub-ADC with two comparators and control logic circuits, DAC, and switch transistors. The sampling capacitor C_1 is divided into C_{1a} and C_{1b}, and C_3 is divided into C_{3a} and C_{3b} for the internal reference generation. The output of the 1st stage cyclic ADC is connected to the input of the 2nd stage cyclic ADC by the switching pulse Φ_{SB}. As described later, the capacitance size of 2nd stage cyclic ADC is designed smaller than that of the 1st stage cyclic ADC.

In the each cyclic ADC, the operation process is as follows: 1) a sampling signal is multiplied with the gain of two, 2) it is then subtracted by the reference voltage determined by the sub-ADC output, 3) next the ADC outputs the digital code, and 4) finally the amplified output signal is returned to the input terminal of the ADC. This feedback cycle is repeated until the required bit resolution is obtained. In our design, the 1st stage cyclic ADC operates four cycles, and the 2nd stage cyclic ADC operates eight cycles, in total 12-bit ADC resolution is obtained.

B. Timing Diagram and Operation

Fig. 4 shows a timing diagram of the two horizontal periods. The horizontal scanning time is 1.92µs at the frame rate of 120 fps with 4336 vertical lines. RT and TX represent control signals for reset transistor and a transfer gate in the pixel, respectively. Analog CDS cancels reset noise in the pixel output signal.

The cyclic ADC has four operation phases: 1) reset, 2) signal sampling, 3) amplification and 4) feedback.

All capacitors in the 1st stage cyclic ADC are initialized with reset phase to remove the residual charge. Then the output signal from the CDS is sampled in the 1st stage cyclic ADC with signal sampling phase, and the sub-ADC generates a three state digital code of the most significant digit. After the signal sampling phase, amplification phase and feedback phase are repeated for three cycles to obtain the first 4-bit resolution. During the amplification phase of the last cycle, 1st stage cyclic ADC is connected to 2nd stage cyclic ADC. (Switch pulse Φ_{SB} in the Fig. 3 is turned on).

Fig. 5 shows the moment that the analog output signal

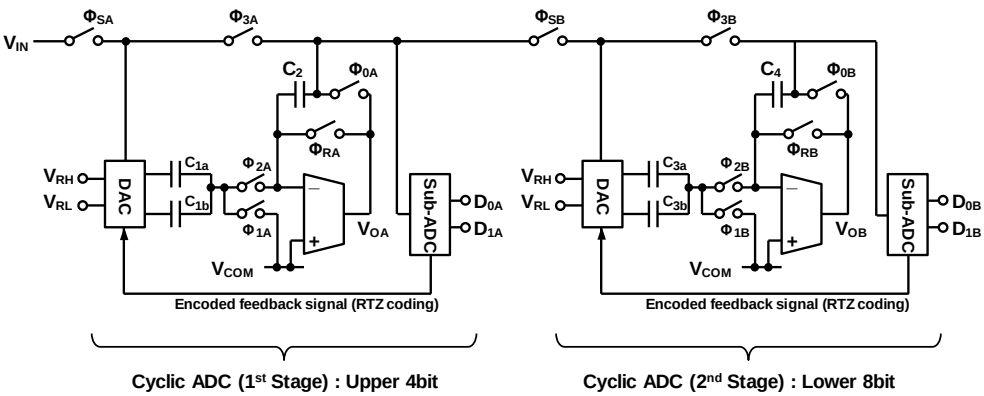

Fig. 3. Simplified schematic diagram of two-stage column-parallel cyclic ADC.

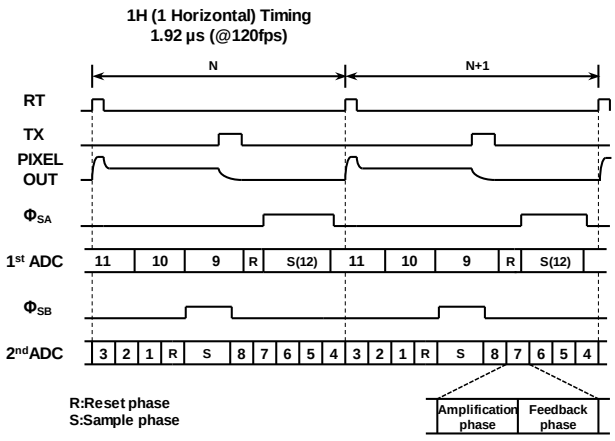

Fig. 4. Timing diagram of two-stage cyclic ADC.

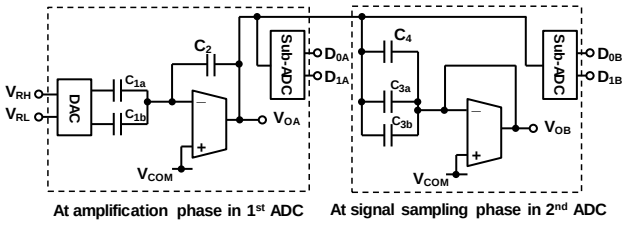

Fig. 5. Signal diagram describing a moment switch pulse Φ_{SB} in Fig. 3 is turned on. Analog output signal from 1st stage cyclic ADC is input to 2nd stage cyclic ADC and sampled with signal sampling phase.

from the 1st stage cyclic ADC is input to the 2nd stage cyclic ADC and sampled with the signal sampling phase. After this signal sampling phase, the switch pulse Φ_{SB} in the Fig. 3 is turned off and the 2nd stage cyclic ADC is disconnected from the 1st stage cyclic ADC. Thanks to this architecture, while the 2nd stage cyclic ADC processes for the rest of 8-bit conversion, the 1st stage cyclic ADC can sample and convert the next pixel signal, which means these two ADCs can process in parallel.

C. *Power Consumption Reduction Effect*

The two-stage cyclic ADC was designed with low-power consumption by exploiting the amplifier function of the cyclic ADC.

A large percent of the power in each cyclic ADC is consumed in the operation amplifier. Slew-rate of the operation amplifier is given by

$$SR = \frac{I_{SS}}{C_L} \tag{1}$$

where I_{ss} is a bias current of the operation amplifier and C_L is a load capacitance. A smaller C_L gives a smaller I_{ss} at the same slew-rate. Because the analog signal output of the 1st stage cyclic ADC is multiplied by 2^N when it processes N-bit, the 2nd stage cyclic ADC needs only (12-N)-bit precision, here 12 is a total bit precision. Thus, it enables the capacitor size of the 2nd stage cyclic ADC to be decreased.

The total current of the two-stage cyclic ADC was estimated by assuming that the capacitor size of the 2nd stage cyclic ADC could be reduced to $1/2^N$ that of the 1st stage cyclic ADC, and the load capacitance of the 1st stage cyclic ADC is C_1 in Fig. 3. The total current of the two-stage cyclic ADC is given by

$$I_{ALL} = m\frac{C_1 V_s}{t_{1H}} \cdot 2N + m\frac{C_1 V_s}{2^N t_{1H}} \cdot 2(12-N) \tag{2}$$

where t_{1H} is the one horizontal time and V_s is maximum output voltage range. The slew-rate limited portion of the settling time is set to 1/m, where m is the arbitrary value. Fig. 6 shows the estimated total current as a function of processed bit number in 1st stage cyclic ADC. In Fig. 6, C_1 equals 1pF, V_s equals 1V, and t_{1H} equals 1.92 µs. Arbitrary value m is set to 4, 5, and 6. When N, which is the process bit number of 1st stage cyclic ADC, is from 2 to 4, the total current of the two-stage cyclic ADC is about one third that in the case of N equaling 12 in which the single cyclic ADC processes 12-bit. In our ADC design, we set N to 4 considering layout area, because larger N gives a smaller capacitor size of the 2nd stage cyclic ADC.

The SPICE simulation was also performed for the designed circuit to estimate the power consumption and compare it with that of a previously reported cyclic ADC [5]. According to the results, though the processing speed of the ADC with 12-bit precision was 1.56 times higher using two-stage architecture, the power consumption was one third that of conventional cyclic ADC.

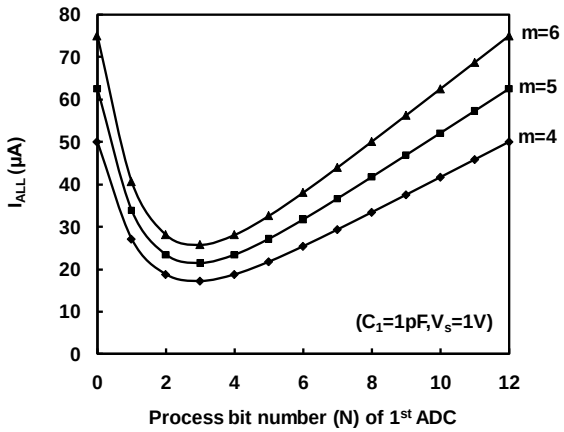

Fig. 6. Simulated total current of two-stage cyclic ADC relative to process bit number of 1st ADC.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

The prototype image sensor was fabricated using a 0.18-µm 1-poly 4-metal CIS process. Fig. 7 shows the die micrograph of the fabricated sensor. The chip die size is 26.5 mm (H) × 21.2 mm (V). In general, horizontal readout routing for these large-format and high-speed image sensors is a difficult challenge. In our image sensor, parallel LVDS driver blocks are placed near the horizontal scanners to reduce the wiring length of the data transfer

path, so as to avoid the degradation of the horizontal readout signals of CML that is performed with a 66MHz double data rate clock.

Table I lists the design specifications of the 33-megapixel CMOS image sensor. The CDS circuit has a programmable gain amplifier function to set the gain ×1, ×2, ×3.5, and ×8. The data rate of each LVDS output port is 533 Mbit/s, and the sensor has an aggregate data rate of 51.2 Gbit/s. The power consumption of the image sensor is estimated to approximately 2.5 W.

Fig. 8 shows an example of the ADC signal waveform that represents input and output of the ADC. The upper wave form is the ADC input signal, which is a 120 Hz sinusoidal signal. The lower waveform represents the digital output that was A/D converted at 120 fps in the sensor, and then D/A converted using external D/A converter to observe on the waveform monitor. Fig. 9 shows a part of the image captured and reproduced from the prototype image sensor.

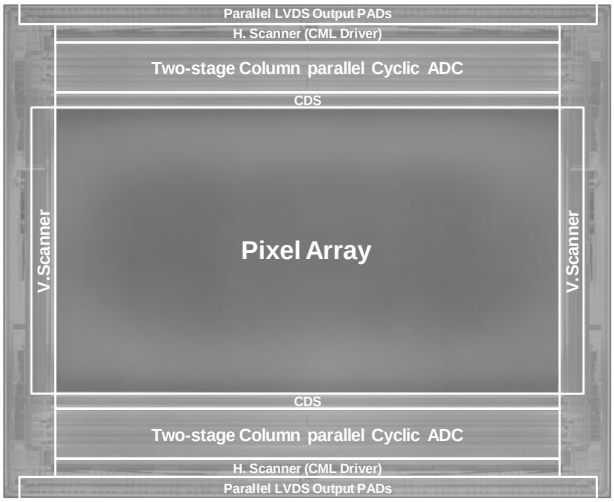

Fig. 7. Die photograph of prototype image sensor .

TABLE I
Design specifications of 33Mpixel CMOS image sensor

Process	0.18 µm 1P4M
Chip size	26.5 mm (H) x 21.2 mm (V)
Power supplies	1.8 V (Digital), 3.3 V (Analog)
Number of active pixels	7680 (H) x 4320 (V)
Number of total pixels	7808 (H) x 4336 (V)
Pixel size	2.8 µm x 2.8 µm
Pixel type	2.5-TR two-shared pixel (Pinned Photodiode)
Frame rate	120 fps
Optical format	3/2 inch
Shutter	Rolling shutter
Gain	× 1, × 2, × 3.5, × 8
ADC	Column-parallel two-stage cyclic ADC
ADC resolution	12 bit
Output interface	96 parallel LVDS
Output data rate	533 Mbps
Package	896 pin BGA
Power consumption	Approx. 2.5 W

V. CONCLUSION

We have designed and developed a 33-megapixel, 120-fps CMOS image sensor with two-stage column-parallel cyclic ADCs. The two-stage column-parallel cyclic ADC effectively reduced not only the A/D conversion time but also the total power consumption. We estimated by a circuit design simulation that the proposed ADC had lower power consumption and faster processing speed than the conventional single stage cyclic ADC. The prototype image sensor with 2.8 µm × 2.8 µm pixel pitch, 7808 × 4336 pixels was developed using 0.18µm 1-poly 4-metal CIS process, and driven at the frame rate of 120fps.

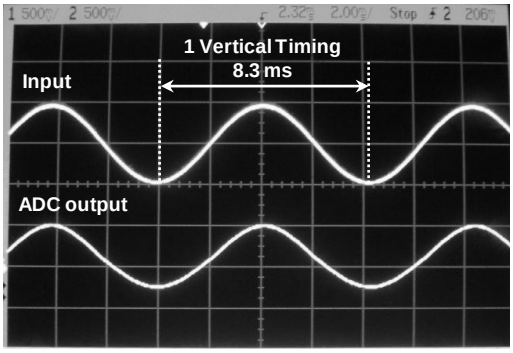

Fig. 8. Operation of two-stage cyclic ADC at 120 fps using 120 Hz sinusoidal input.

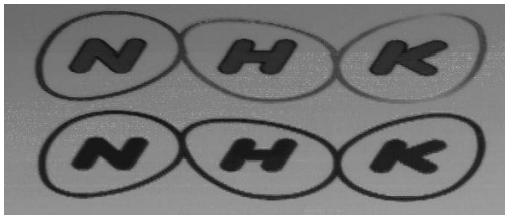

Fig. 9. Part of image reproduced from prototype image sensor.

REFERENCES

[1] I. Takayanagi, et al., "A 1.25-inch, 60-Frames/s, 8.3-M-Pixel Digital-Output CMOS Image Sensor" , IEEE J. Solid-State Circuits, vol. 40, no. 11, pp. 2305-2314, Nov. 2005.

[2] I. Takayanagi, et al., "Progress in 1.25-inch Digital-Output CMOS Image Sensor Developments for UDTV Applications", Proc. 2009 International Image Sensor Workshop, pp.304-307, 2009.

[3] T. Yamashita, et al., "Experimental color video capturing equipment with three 33-megapixel CMOS image sensors", Proc. IS&T/SPIE Electronic Imaging, February 2009.

[4] S. Huang, et al., "A 2.5 inch, 33Mpixel, 60 fps CMOS Image Sensor for UHDTV Application", Proc. 2009 International Image Sensor Workshop, pp.308-311, 2009.

[5] J. -H. Park, et al., "A High-Speed Low-Noise CMOS Image Sensor With 13-b Column-Parallel Single-Ended Cyclic ADCs", IEEE Trans. Electron Devices, Vol. 56, No. 11, pp. 2414-2422, Nov. 2009.

[6] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166–172, Mar. 1995.