A 26.2Mpixel, 74fps, Global Shutter CMOS Imager with 20Gb/s Interface for Multi Object Monitoring

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***Abstract*—Current developments in CMOS imagers favour higher resolutions, increasing pixel rates [1] and on-chip configurability. This paper presents a 25.5 mm x 32.5 mm sized CMOS imager targeted for high-end machine vision industry featuring pipelined global shutter. This reconfigurable operating mode imager is composed of 5120 x 5120 5T pixels with pinned photodiodes on 4.5 μm pitch. Up to 32 regions of interest can be programmed in the sensor. The high level of configurability in conjunction with high speed readout enables the possibility to monitor multiple moving objects.**

I. Introduction

Sixty-four 10 bit A/D converter outputs are multiplexed to thirty-two 10 bit serial LVDS output channels reaching an aggregate datarate of 19.84 Gb/s at 74 frames per second at full resolution. Higher frame rates can be achieved using windowed or 2x2 pixel binned readout modes. The sensor features 128 busses that run over the full width of the chip enabling fast windowing modes. In architectures with column parallel A/D converters [2], the line rate is fixed, and only changing the Y-dimension of the window helps to increase the frame rate. The benefit of the proposed architecture is that the pixel rate is kept constant while it is possible to increase the frame rate by reducing the Y- and X-dimensions of the window.

II. Architecture

The chip block diagram is shown in figure 1. The image core consists of a pixel array including driver circuits. The analogue pixel signals are sampled on 5120 column Sample&Hold structures (S/H) and connected via 23 mm busses to the 64 programmable amplifiers as shown in figure 2. Such wide busses challenge RC limits and may lead to excessive substrate noise on large die imagers. Therefore, a fully differential signal chain is implemented starting from the column. Moreover, the voltage swing on the busses is reduced despite the disadvantages this has for the noise performance. While the 10 bit ADC outputs are being processed to 10 bit serial LVDS data streams, frame synchronisation codes such as frame start, line start, frame end and line end indications, are routed to a dedicated LVDS channel. This configuration allows to minimise the overhead as compared to typical 8b/10b encoding

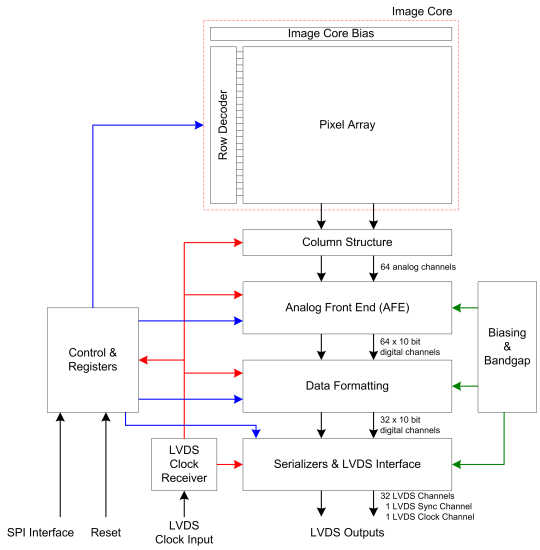

Fig. 1. Block Diagram of the Image Sensor

schemes and allows for easier separation between control and data flow in the sensor. This synchronisation channel also contains information about the region of interest being processed, facilitating the image reconstruction at the receiving end.

III. Global Shutter

In a global shutter, image capture takes place on all pixels concurrently although the subsequent readout is sequential. With shutter times less than 50 μs, global shutter operation on this large format pixel array with dimensions of 5.3 cm^2 puts special constraints on the power distribution for the pixel drivers. In less than 50 μs more than 30.000 pixel drivers need to switch on and off again with uniform timing and without leaving a trace in the substrate. Dedicated power strapping for the pixel drivers reduces IR drop. After integration, all pixel values are sampled on the storage node inside the pixel. Integration of the next frame occurs concurrently with the readout of the current frame. As global integration operations

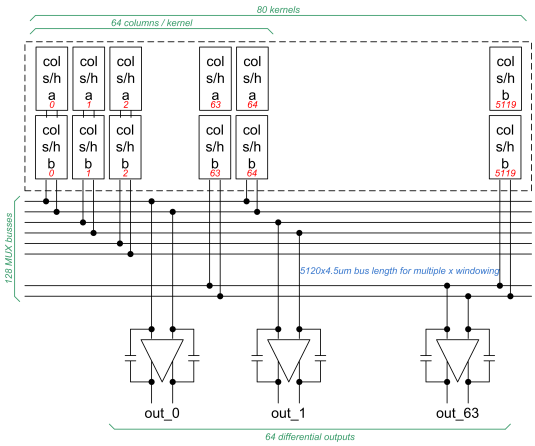

Fig. 2. Column Multiplexer Supporting Zero ROT Readout Mode

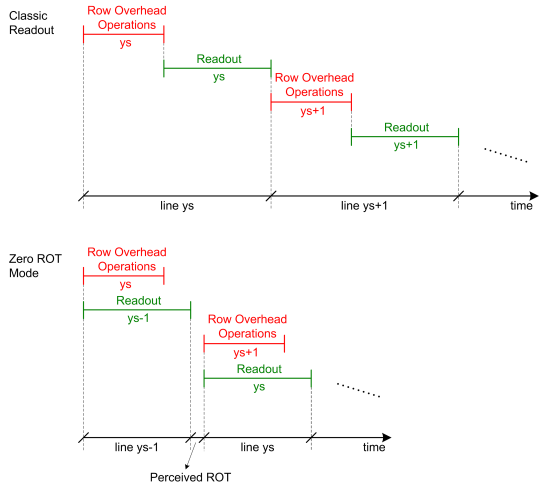

Fig. 3. Illustration of Classic and Zero ROT Readout Mode for Two Lines

may affect the read-out of the signals stored in the array, indirectly through the substrate, and directly through IR drop in the pixel supplies, these operations are carefully scheduled while the readout is temporarily put on hold.

IV. Zero Row Overhead Time

To reduce the total line time, a zero row overhead time (Zero ROT) mode is implemented by using two S/H banks. By alternatively addressing the two banks, the row operations and kernel readout can be performed at the same time. To support double sampling each bank contains two capacitors. The pixel's reset value is sampled on capacitor C_r, while the pixel's signal value is sampled on the capacitor C_s. In zero ROT operation mode, the column S/H capacitor $C_{r,a}$ and $C_{s,a}$ are charged with new pixel values, while the second bank, $C_{r,b}$ and $C_{s,b}$, are being read out and vice versa, as shown in figure 2. The actual row operations may be longer, however the perceived ROT is shorter as depicted in figure 3. With the use of zero ROT mode frame rate increases of 40% can be achieved while keeping the input frequency constant.

V. Windowing

Up to 32, possibly partially overlapping, windows can be configured and read out in global shutter mode. The exposure and window parameters can be updated dynamically without interrupting the image capture process. A separate register indicating the subset of active windows can be used to track moving objects. As illustrated in figure 4, a moving object can be tracked by defining five partially overlapping windows. In order to minimise the impact on the frame rate, only the centre window is active, while four surrounding windows are pre-programmed in the sensor. The direction of movement can be detected by subtracting subsequent images. Based on this analysis, the host enables the pre-programmed window to which the object is moving (i.e. window #3 in the illustration). As this is achieved by updating only one register, the impact on the inter-frame time is minimised. During the readout of the following frame, the inactive windows are repositioned such that the new configuration reflects the initial state. Multiple objects can be tracked by defining multiple sets of windows as described above. The size of the active window(s) determine the maximum frame rate at which the sensor can be operated. This may be traded off with the required window repositioning frequency and the maximum speed at which the objects need to be tracked.

There may be some ambiguity with choosing the correct direction when the object is moving in a perfect horizontal or vertical direction. Suppose, in the previous example, that the object is moving to the right. In this case the system can equally choose window #2 or window #3 as new active window. However, in subsequent decisions, the system may be oscillating between the upper or lower windows. To avoid this oscillation, one could define four extra windows, as shown in figure 5. In the example given, the new active window would be window #6. An extra advantage of this configuration is that it allows monitoring of faster moving objects, as the surrounding windows cover a larger area. One can see that the inactive windows form a better circle around the object. Obviously, the disadvantage is the fact that more windows need to be programmed, which puts an upperlimit to the total number of objects simultaneously monitored by the sensor.

VI. Conclusion

In conclusion, the reported sensor achieves data rates of almost 20 Gbit/s with comparable energy and area efficiency as reported in [4]. To the authours' knowledge, this is the largest resolution, single chip sensor with snapshot shutter. At a pixel rate of almost 2 Gpixels/s the sensor consumes 3.5 W. Seamless multiple object tracking with increased frame rate is achieved with the on chip configurable sequencer, which is not possible with the architecture as proposed in [2]. The modular channel design approach makes it easy to scale this sensor to smaller resolutions with comparable optical performances suitable for many new applications amongst machine vision and monitoring industry. Figure 6 shows a sample image taken at full resolution. A micrograph of the imager, packaged in a 355 pin μpga is shown in figure 7.

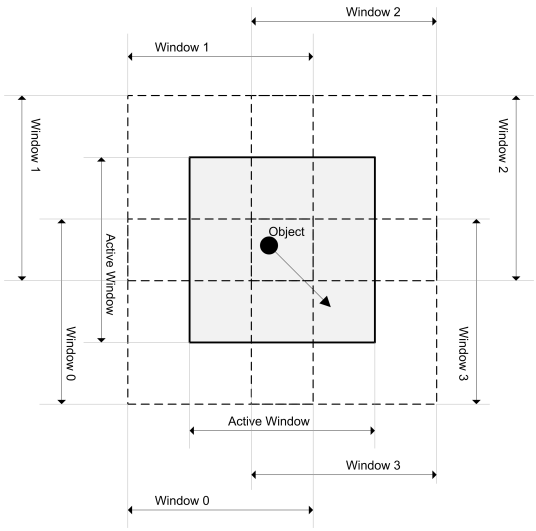

Fig. 4. Multiple Window Motion Tracking with 5 Windows

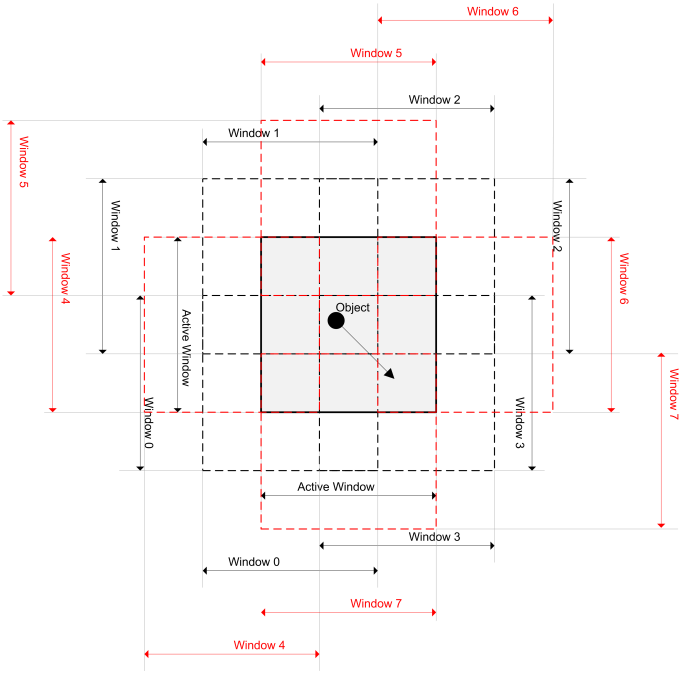

Fig. 5. Multiple Window Motion Tracking with 9 Windows

References

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Fig. 6. Prototype Sample Image

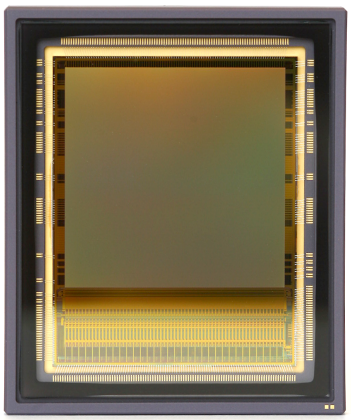

Fig. 7. Imager Micrograph