A 768x576 Logarithmic Image Sensor with Photodiode in Solar Cell mode

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ABSTRACT

The wide dynamic range and the contrast indexed imaging of logarithmic sensors have a great interest for a large variety of applications from digital photography to automatic machine vision. Still today, the high fixed pattern noise, low sensitivity and image lag remain open in such designs. In this paper, we present a new logarithmic pixel design by using photodiode in solar cell mode. This pixel design has been successfully integrated into a 10um pitch 768x576-pixel CMOS sensor in a standard 0.35um technology and demonstrated an ultra low fixed pattern noise, high sensitivity and absence of image lag. The useful instant dynamic range has been measured superior to 120dB.

GENERAL PRINCIPLE AND STRUCTURE OF THE SENSOR

All the biological sensory functions follow logarithmic law. The fundamental advantage is the ratio metric response of a logarithmic law sensor. In imaging field, this property results in a contrast indexed image and very wide instant dynamic range. The early work on logarithmic sensors has been based on logarithmic current to voltage converting circuit using mainly MOS in sub-threshold mode [1-7]. Fig. 1 gives a principle schematic of such pixel design. But this kind of pixel designs cannot offer high quality image for general purpose imaging applications despite of years of R&D effort. The high fixed pattern noise, low sensitivity and image lag are the main obstacles.

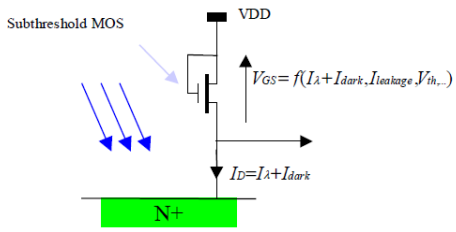

Figure 1. Traditional CMOS logarithmic pixel structure where the linear mode photo current is converted into a logarithmic voltage by a sub threshold mode MOS transistor.

Inspired by the knee response in a CCD under blooming state, we have tested a photoreceptor design by using a photodiode under blooming state (solar cell mode) in order to get a logarithmic law signal from the photoreceptor[8]. The cross-talk issue has been resolved by using the P+ diffusion photodiode in a separate Nwell. This structure has given a good logarithmic law signal in function of illumination over more than 120dB dynamic range. But the quantum efficiency was poor and suffered from large image lag too. New pixel design with N-in-Psub photodiode has been developed since. A 160x120-pixel test chip for concept validation has been published [9].

Fig. 2 shows the basic electrical schematic of this newly developed logarithmic pixel. The photodiode working in solar cell mode is made with N diffusion in P-sub. A zeroing NMOS transistor crosses this photodiode and shorts it when it's on. The negative photovoltaic voltage on the cathode of the N-in-Psub photodiode is translated into a positive one by the in-pixel PMOS voltage follower. A differential readout is realized in order to remove the additive FPN noise in the sensor readout chain as in a classic APS sensor.

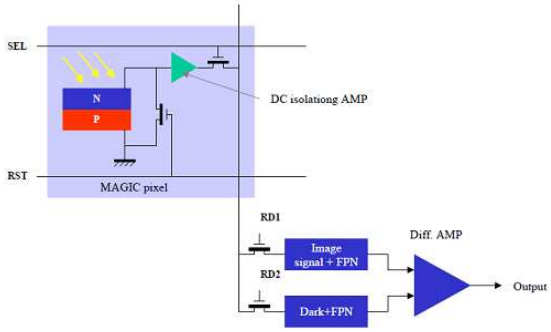

Figure 2. New logarithmic pixel design by using a photodiode in solar cell mode. The open-circuit voltage of the photodiode is sensed and a short-circuit MOS gives a precise dark reference signal for FPN compensation and also lag suppression.

Fig. 3 illustrates the global architecture of this sensor. This sensor has been designed initially for analog surveillance camera, so no AD converter is integrated on-chip. Instead a CCIR/EIA TV encoder is integrated on-chip which permits a direct generation of the composite video signal from the sensor. Thanks to the huge dynamic range of this logarithmic response, no exposure and no AGC are needed. The circuit design is relatively simple. All the control signals are provided by an off-chip controller, either a micro controller or a FPGA.

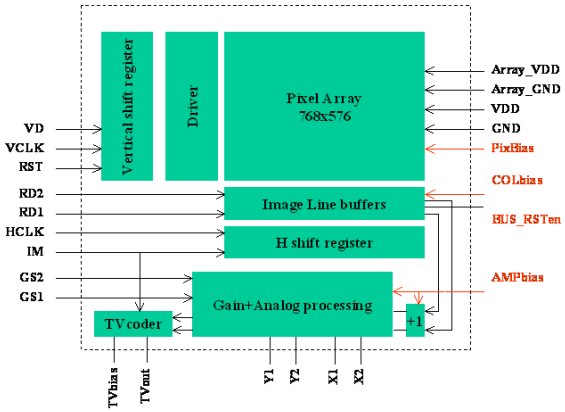

Figure 3. The general structure of this 768x576 logarithmic CMOS sensor with on-chip CCIR/EIA encoding circuit.

Pixel lines in the array are sequentially selected by the vertical shift register. RD1 signal loads the image signal from the selected line into a first analog buffer. Then RST signal activates the zeroing transistor which short-circuits the photodiode and at the same time RD2 signal loads the zero voltage signal into a second analog buffer. The photodiode zeroing action gives not only a precise FPN compensation reference signal but also removes the image lag due to the residual charge on the photodiode.

The difference between the two readout results gives a FPN compensated image which is output in a differential format. This differential image signal goes back into the CCIR/EIA encoder circuit. The video signal is amplified and mixed with TV synchronization pulse and black level. The composite TV signal will be available on the TVout pin. The sensor is powered with a 3.3V supply. The current drain is about 80mA. Fig. 4 shows some high contrast scenes captured by this sensor. For the characterisation purpose, we have built a CameraLink based camera board operating at 25 images per second. The differential output of the sensor is connected to a differential ADC. The AD conversion range is set at 1V with 12-bit precision.

Figure 4. Some high dynamic range scenes captured by the sensor.

The main characteristics and performance of this sensor are summarized in Tab. 1. In the following sections, we will focus on the measured results together the theoretical modelling of this pixel design.

PHOTOELECTRIC RESPONSE

The open-circuit voltage of an illuminated photodiode in its steady state can be simply calculated from Shockley equation:

$$V_D = \frac{kT}{q}\ln\left(\frac{I_\lambda + I_s}{I_s}\right) \qquad (1)$$

where k, T, q, I_S and I_λ represent respectively Boltzmann constant, absolute temperature, elementary charge, junction saturation current and photo current.

In our design, the photodiode's open-circuit voltage is established progressively from zero voltage after the zeroing action. The duration of the establishment depends on illumination level and also exposure time. If the voltage is sampled before the fully established state, it can be deviated from the log law given by Shockley equation. By supposing a constant value C_D for the junction capacitance, we can get a closed form response for the photodiode in function of photo current (illumination) and exposure time t:

$$V_D = V_T \ln \frac{I_\lambda + I_s}{I_\lambda e^{-\frac{(I_\lambda + I_s)t}{V_T C_D}} + I_s}, \text{ where } V_T = \frac{kT}{q} \qquad (2)$$

From this analysis, we can see that the pixel response will be linear at low illumination level or at short exposure time. A very good match has been observed between the theoretical model and the measured data (Fig. 5). So the constant junction capacitance hypothesis is held thanks to the small voltage excursion on the solar cell mode photodiode.

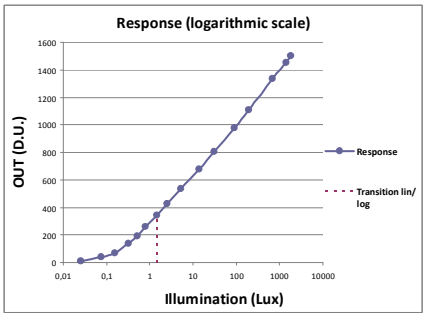

Figure 5. Measured sensor response in function of faceplate illumination level at 25fps (D.U. =0.25mV).

RANDOM AND FIXED PATTERN NOISES

When the photodiode operates in logarithmic region, the random noise on the photodiode is simply a Johnson noise. Due to the junction capacitance and also parasite capacitance on the photodiode, the voltage seen by the readout amplifier is basically a RC filtered white noise. By integrating over the whole bandwidth, we have the random noise:

$$v_n^2 = 4kTR_D B = 4kTR_D\left(\frac{1}{4R_D C_D}\right) = \frac{kT}{C_D} \qquad (3)$$

where R_D is the junction dynamic resistance

When the photodiode is still in linear (integration) mode, the random noise will be composed of two components: one is the KT/C noise due to the zeroing transistor cutoff and also the additional photon noise:

$$v_n^2 = \frac{kT}{C_D} + \frac{Nq^2}{C_D^2} \qquad (4)$$

where N is the accumulated photoelectron number

Theoretically we should be able to see a noise level peak around the linear to log transition. The measured results show that this shot noise contribution is marginal and can be ignored. By consequent, we can reasonably conclude that the random noise is constant over all the operation range. The fixed pattern noise after the on-chip compensation is low and not noticeable by eye. We can still observe some column FPN. The measured FPN in function of illumination as shown in Fig. 6 increases linearly with the image signal (logarithmically with the illumination level). We think that the FPN comes mainly from the additive offset voltages in the readout chain. The residual FPN is caused by the non-linearity of the amplifiers and also of the MOS capacitors because neither PIP nor MIM capacitors have been used. So there is still room for further improvement.

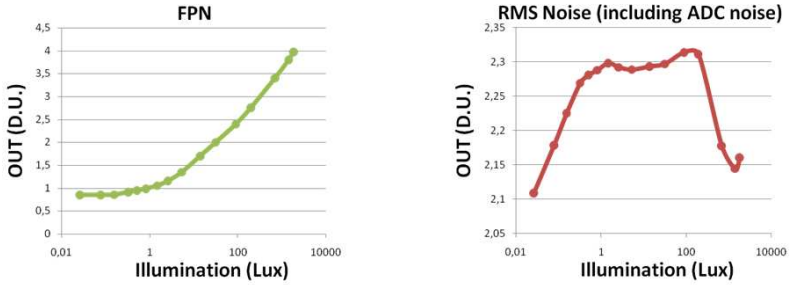

Figure 6. Measured random noise and FPN at 25fps under different illumination level (D.U.=0.25mV)

CONCLUSION

In this paper, we have presented a 768x576 logarithmic CMOS image sensor by using photodiode in solar cell mode. By using this innovative pixel design, we have drastically reduced the fixed pattern noise, eliminated the image lag and improved the sensitivity. This logarithmic CMOS sensor design has reached the performance of a good quality 3T APS sensor in terms of noise, fixed pattern noise but with an instant dynamic range better than 120dB which exempts the sensor from any exposure control. The further work will be on the pixel size reduction, resolution improvement and especially the noise reduction.

Pixel Size	10umx10um
Fill Factor	30% on layout
Photodiode structure	NWell in Psub photodiode
High light Log sensitivity	90mV/decade
Low light linear sensitivity	3V/lux*s @ 25fps
Random Noise	0.5mV over all DR
Fixed Pattern Noise	< 1.5mV
CMOS process	Standard 0.35 1P3T CMOS process
Resolution	768x576
Maximum H scanning rate	> 35Mhz
Power consumption	80mA @ 3.3V

Table 1. Sensor's characteristics and performance summary.

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