Paper Number: R26

An Autonomous micro-Digital Sun Sensor Implemented with a CMOS Image Sensor Achieving 0.004º Resolution @ 21mW

Ning Xie[1], Albert J.P. Theuwissen[1, 2], Bernhard Büttgen[1, 3]

[1]Delft University of Technology, Delft, the Netherlands; [2]Harvest Imaging, Bree, Belgium; [3]MESA Imaging, Zürich, Switzerland.

Email: n.xie@tudelft.nl

Abstract

The micro-Digital Sun Sensor (μDSS) is a sun detector which senses a satellite's instant attitude by detecting its attitude angle with respect to the sun**.** It is composed of a solar cell power supply, a RF communication block and an imaging chip, which is called APS+. The APS+ integrates a CMOS Active Pixel Sensor (APS) of 368×368 pixels, a 12 bit Analogue to Digital Converter (ADC), and digital signal processing circuits. This paper describes the implementation of a prototype of the μDSS APS+ fabricated in a standard 0.18μm CMOS process. The APS+ is particularly characterized by its low power consumption (a factor 10 lower compared to the state-of-the-art) since power is a critical specification for space application. The power is mainly reduced by "profiling" and "windowing", which are enabled by a specific active-pixel design. The measurement results are discussed following in this paper.

I. Introduction

The μDSS [1] is basically a pinhole camera. The working principle is depicted in **Error! Reference source not found.**. The CMOS image sensor is placed on the satellite, with a membrane above its focal plane. The pinhole is located at the center of this membrane. The sun light passes through the pinhole and projects an image on the CMOS image sensor's pixel array. By reading out the centroid of the sun light projected image, the sunlight incident angle (θ) can be calculated. Furthermore the satellite's attitude can be determined according to the sun light incident angle.

Figure shows the overall architecture of the μDSS. It is composed of an imaging chip named APS+, a solar cell, and an RF module. The APS+ consists of an APS, a chip-level ADC and a digital processing circuit. The latter consists of a timing and control signal generator, a centroid algorithm circuit, and an I/O interface.

II. Working principle

As indicated in Figure , the size of the sun spot on pixel array is approximately 10×10 pixels, which is much smaller than the size of the complete pixel array (368×368 pixels). Therefore windowing could be a good readout option for power reduction. The APS+ adopts a power saving two step acquisition - tracking readout method. Once powered on, the APS+ works in the sun acquisition mode in order to detect the coarse location of the sun spot. At the end of the acquisition, the APS+ determines a Region of Interest (ROI) by evaluating the intensity profiles in column and row directions. In the next step, the APS+ starts working in sun tracking mode: all pixels in the ROI are readout and the final centroid is extracted by the digital algorithm.

III. Low power approach

Some previous digital sun sensors have already adopted the acquisition-tracking readout method [2]. However the power consumption in acquisition mode could be more than 1.5 times higher than in the tracking mode since the complete frame has to be scanned in the existing solutions.

The APS+ consumes much lower power in the acquisition mode by a profiling method. The profiling is enabled by a specific pixel design,

as illustrated in Figure 3(a). This pixel is designed based on 3-T APS pixel, however with an extra column select transistor (CS). The pixel implements a "Winner-Takes-It-All (WTIA)" principle [3]. The timing diagram is illustrated in Figure 3(b). When "column/row profile" is active, all pixels in the array are selected and the pixels on respective column/row are shorted. At the end of the integration time, every column/row bus of the image sensor holds the information of the most heavily illuminated pixel (the "winner") on each particular column/row. In this way, the profile along column/row-direction can be achieved. The measurement result of profiling is presented in Figure 4.

During "row profiling" period, an extra row readout circuit is required in order to read out the voltage on each row. In order to further simplify the readout circuit, the pixel array is modified. The column and row buses are short cut at the positions of the diagonal pixels (as the dots indicate in Figure 3(a)). In this way the row profiling information is shared by both column and row buses. So the row profiling could be read out on the column buses. No extra readout circuit is necessary for row buses anymore.

With the profiling method, column and row profiles are achieved within the readout time for two lines. This short readout time leads to ultra-low power consumption in the acquisition mode, which is 21.34mW @10fps.

IV. Low noise approach

In the sun tracking mode, the final centroid result is extracted. Therefore low noise is the major consideration in this mode. The 3-T pixel structure is required by the WTIA principle. The drawback is that its reset noise is higher than in the 4-T pixel structure. In order to reduce the kTC noise, the APS+ employs a readout strategy called "quadruple sampling". The timing diagram is depicted in Figure 3(c). Four samples are taken in one readout cycle. Samples S1 and S4 are taken when RST is active; S2 and S3 are taken at the beginning and end of integration time, respectively. The kTC noise components in S2 and S3 are correlated, and can be cancelled by subtracting. During the quadruple sampling, firstly the subtractions of S1-S2 and S4-S3 are processed in the analog domain in order to minimize the 1/f noise, and the results are digitally stored on chip. Next, the digital outputs of the previous actions are subtracted in order to cancel the kTC noise. In the end, the final output is (S4-S3)-(S1-S2) = S2-S3. In this result, the 1/f noise and kTC noise, being the major noise contributions, are minimized and cancelled respectively. The measurement result is presented in Figure 5. Both the quadruple sampling and the conventional delta double sampling (DDS) are applied to APS+. It shows that quadruple sampling achieves 15% less thermal noise than DDS.

V. Performance

The working temperature range for the µDSS is specified from -40ºC up to +80ºC. Figure 6 shows the noise level at high temperature normalized to the noise at room temperature of 25ºC.

The comparison between the presented work and other recently reported sun sensors are listed in Table 1. It clearly shows the improvements in power consumption, chip size, accuracy, and resolution. The micrograph of the APS+ is presented in Figure 7.

References

[1] C. W. de Boom, et al, "Micro Digital Sun Sensor: System in a Package", *International Conference on MEMS, NANO and Smart Systems (ICMENS'04),* Alberta Canada, August 25-27, 2004

[2] F. Boldrini et al., "Applications of APS detector to GNC sensors", *4th IAA Symposium on Small Satellites for Earth Observation*, Berlin, Germany, 7 - 11 April 2003.

[3] Ning Xie, Albert J.P. Theuwissen, Xinyang Wang: "A CMOS Image Sensor with Row and Column Profiling Means", *IEEE Sensors 2008 Conference*, Lecce, Italy, pp. 1356-1359, 2008.

[4] Data sheet from Sinclair Interplanetary website: {http://www.sinclairinterplanetary.com/digitalsunsensors/sunsensor2009b(1).pdf}, accessed September 3 2010.

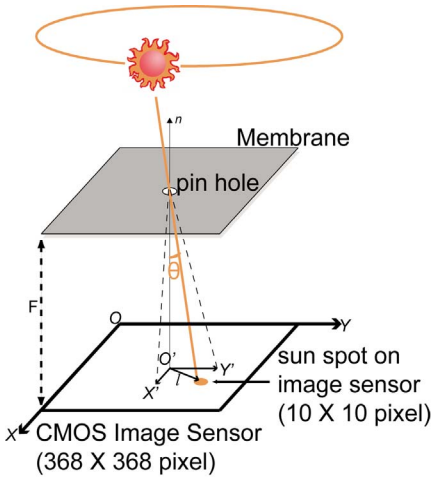

Figure 1 Working principle of the µDSS

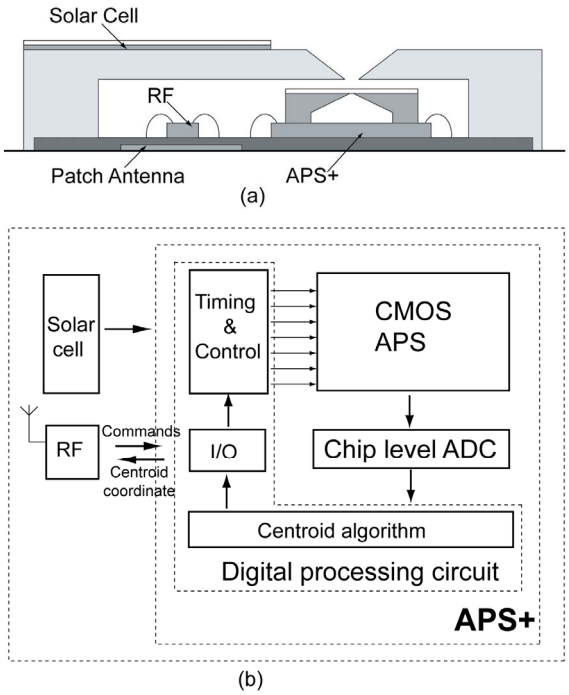

Figure 2 (a) Cross section of the µDSS system; (b) Block diagram

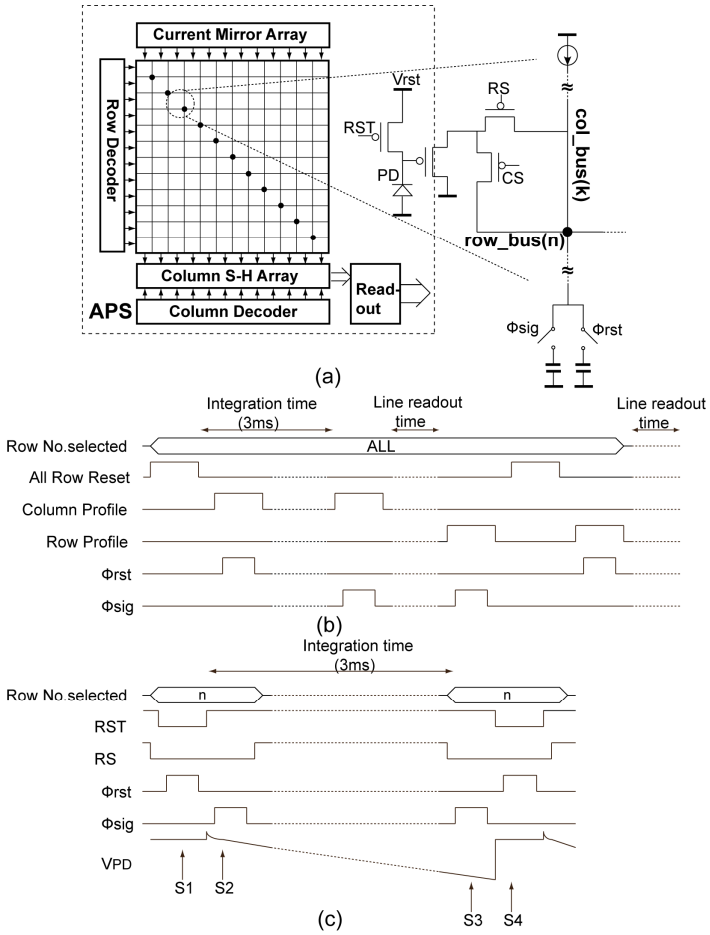

Figure 3 (a) Structure of APS and pixel; (b) timing diagram in acquisition mode; (c) timing diagram in tracking mode

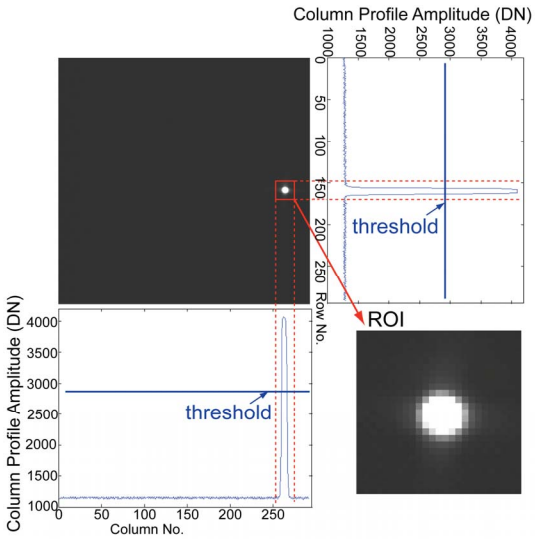

Figure 4 Measurement results from acquisition mode and tracking mode

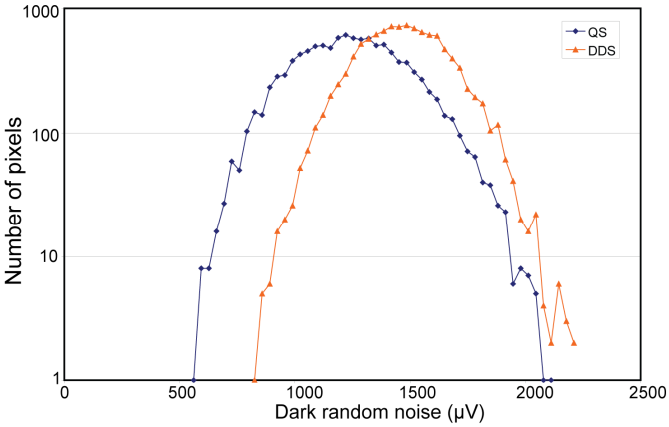

Figure 5 Histogram of dark random noise with Quadruple Sampling (QS) and Delta Double Sampling

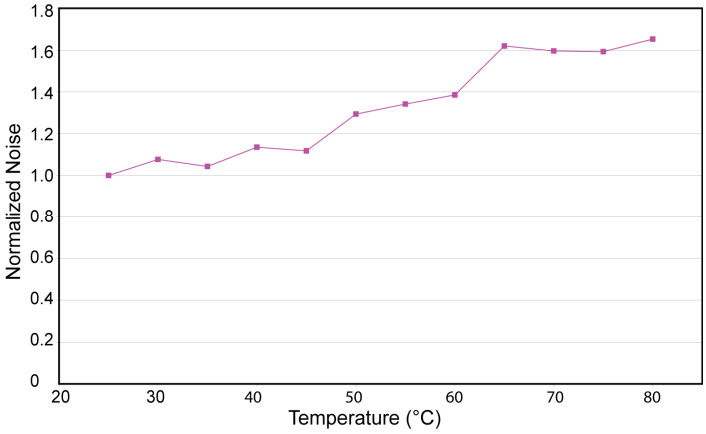

Figure 6 Noise vs. Temperature

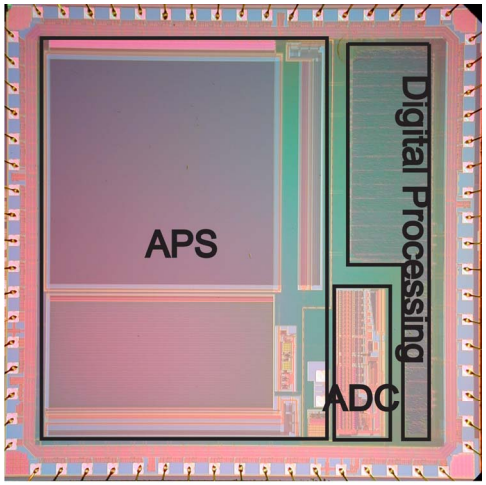

Figure 7 Micrograph of APS+

µDSS vs. counterparts	Characteristic	µDSS (This work)	Galileo (ESA) [2]	SS-411 [4]
	Year	2010	2010	2009
	Chip Size	5mm ×5mm	11mm ×11mm	Not available
	Pixel Array	368 × 368	512 × 512	Not available
	Power Consumption	21.34mW @Acquisition 21.39mW@Tracking	327mW @ Acquisition 193mW @ Tracking	75mW
	Power Supply	3.3V for analog 1.8V for digital	3.3V for analog 1.8V for digital	5V
	FOV	±47º	±64º	±70º
	Operating Temperature	-40ºC to +80ºC	-40ºC to +70ºC	-25ºC to +70ºC
	Accuracy	0.02º (3σ)	0.024º (3σ)	0.11º (2σ)
	Resolution	0.004º	<0.005º	Not available
	Detection Principle	Single pin hole	Single pin hole	Multiple-apertures

Table 1. Performance comparison between the µDSS and the state of the art