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CCD and CMOS combined, low noise and low power dissipation linear image sensor with variable charge mixing mode

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1. Introduction

It is well known that CCD image sensor has very low noise performance but big power consumption, while CMOS image senor has much less power consumption. The SNR of CMOS image sensors are improved year by year remarkably. So in these days, CMOS image sensors overcome CCD image sensors. Nevertheless the fact that CMOS sensor cannot mix signal charge freely as CCD image sensors is still one of their disadvantages. As pixel number is increasing, down scaling becomes more important. To make binning signal data, if signal electrons are able to be mixed, it is basically advantageous to reduce dark noise.

2. CCD and CMOS combined linear image sensor

To make use of advantages both CMOS and CCD sensor, in the case of linear image sensor, CCD and CMOS combined, low power and charge mix image sensor has been developed.

Comparing with CCD and MOS image sensors, CCD and CMOS combined sensor has CCD portion to store and mix signal charge between photodiode and MOS readout circuits (Fig.1).

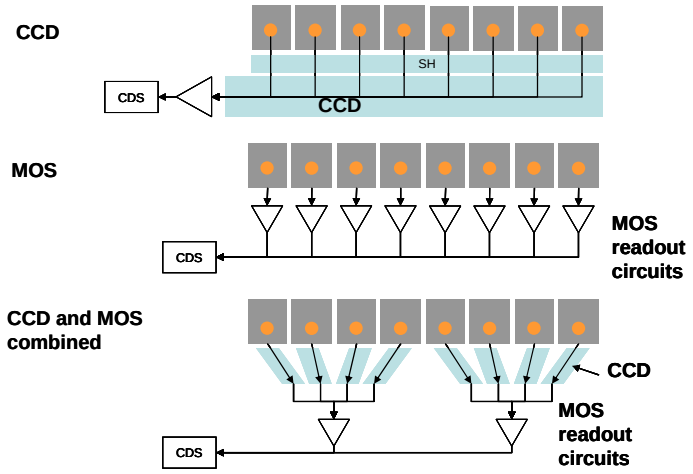


Fig.1 Bock diagram of CCD and CMOS combined sensor

The sensor has 21.16 micro meter pitch 688 pixel array. 15 sensors aligned inline to capture A4 size document in resolution of 1200 DPI (Dots Per Inch) (Fig.2).

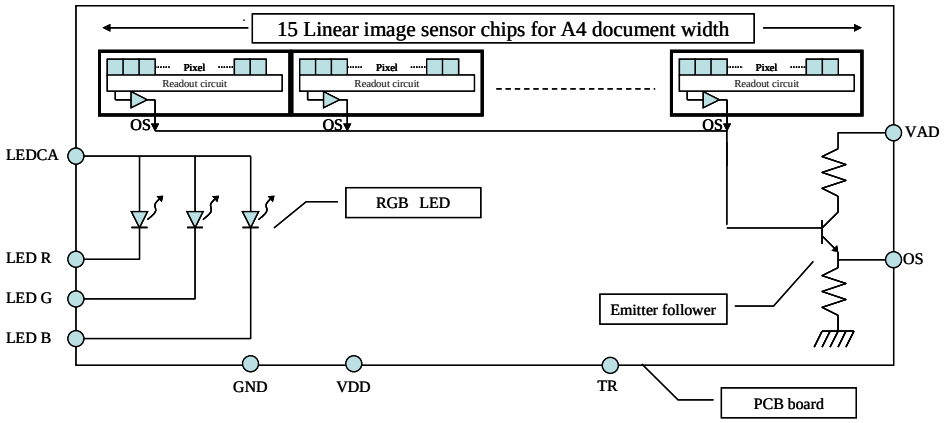


Fig.2 Multi chip image sensor for A4 document reader

One CCD block is located at every 4 photodiodes and can mix 2 or 4 signal charges that correspond to the resolution of 600DPI or 300DPI, respectively (Fig.3).

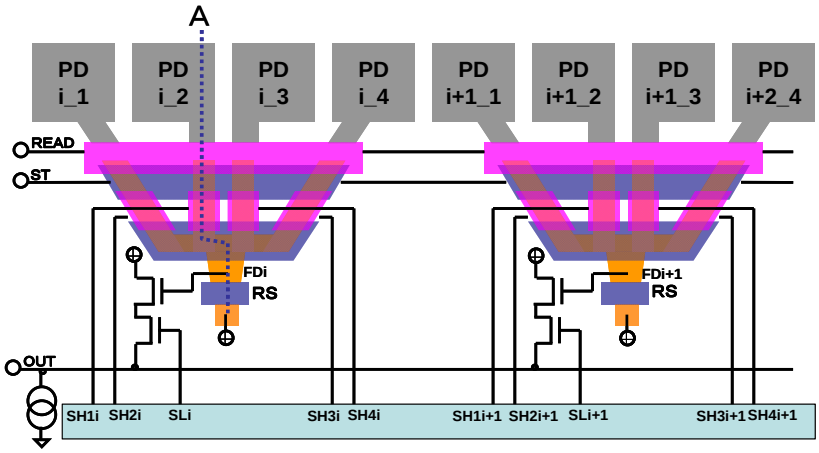


Fig.3 Bock diagram of CCD and CMOS combined sensor

During signal integration period, signal charges are stored in photodiodes (Fig.4,5 t1), and then all signal charges are simultaneously transferred to storage gate (ST, t2). Finally signal charges are transferred by shift gate (SH) to floating diffusion (FD,t3-6) to be converted signal voltage. To readout each signal charge separately, SH gates are drove separately (Fig.5 (2)), and to readout mixed four signal, four SH gates are drove simultaneously (Fig.5 (1)). Charge detection circuits are also put at every four pixels, so circuit area size is diminished.

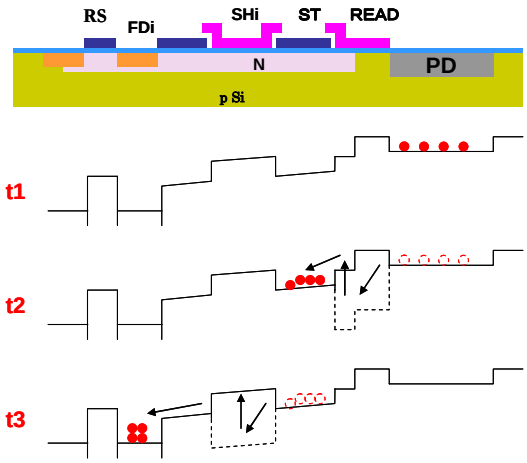
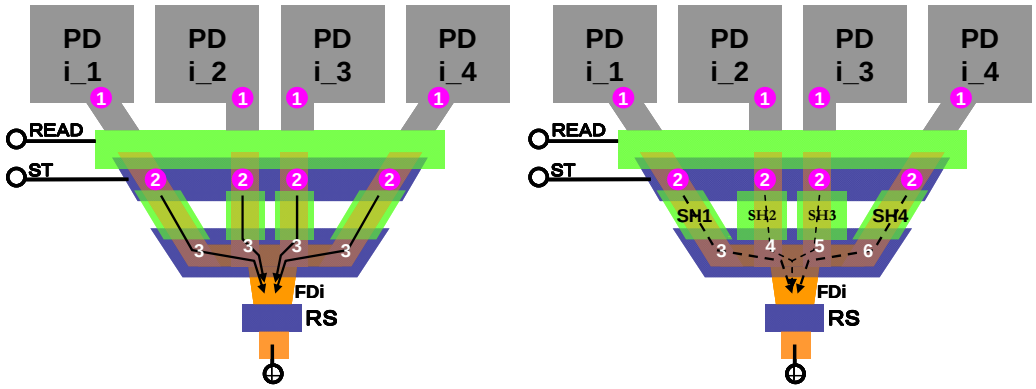


Fig.4 Cross section and potential profile of photodiode and CCD portion

CCD electrodes can be consisted of single layer poly silicon electrodes [1] to simplify manufacturing process and reduce load capacitance of CCD (Fig.6).

In this structure, CCD channels are likely to be long and winding (Fig.7), so to accelerate charge transfer, channel potential is gradually deepened toward charge transfer direction. This potential slope is produced by changing width of charge transfer channel (Fig.8 (a)) or changing impurity concentration of channel [2] (Fig.8 (b)).



(1) 4 mixed mode

(2) none mixed mode

Fig.5 Readout operation

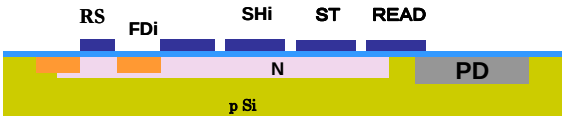


Fig.6 Cross section of single layer CCD

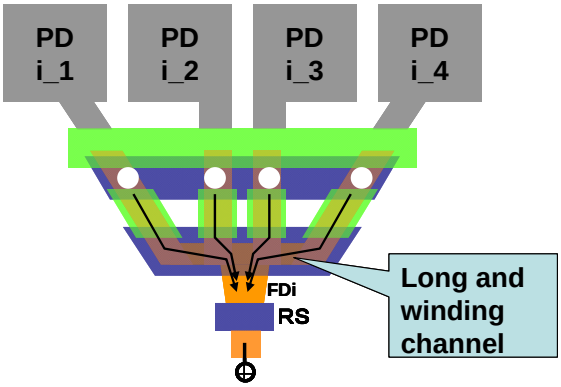
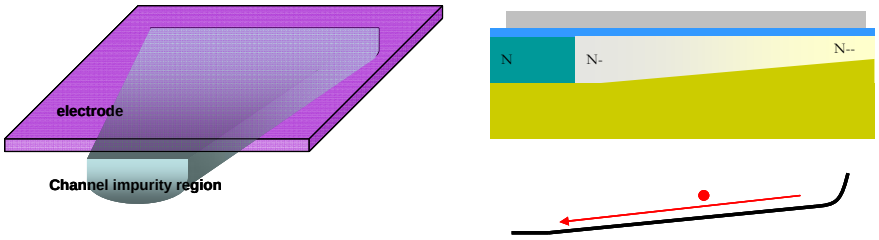


Fig.7 CCD channel path



(a) Potential slope by difference of channel width

(b) Potential slope by difference of impurity concentration

Fig.8 charge transfer acceleration by potential slope

3. Performance

Good output waveforms are obtained both of all pixel readout mode and four signal mixed mode (Fig.9). Their output data rate is 2.5MHz. Power supply voltage is 3.3V and its power dissipation is measured 16.7mW (Fig.10). It is almost the half of CCD sensor that has same specifications. Load capacitances are less than tenth of CCD image sensor (Tabe.1). Furthermore, measured random noise is less than CCD sensor and the value is equal both in non-mix and four mix modes. (If signal is mixed by averaging signal voltage in CMOS sensor, the value will be doubled.)

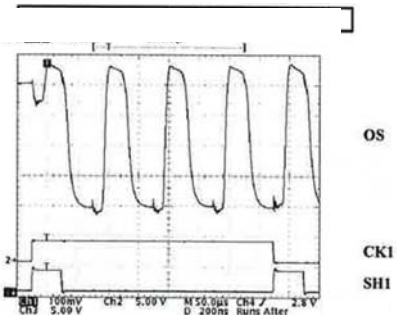
4. Conclusion

Comparing with CCD and CMOS sensor, CCD and CMOS combined sensor overcome the both in almost all aspects (Tabele.2). CCD and CMOS combined structure has possibility to produce novel features for image sensors.

[1]M. Monoi, et al, SPIE Vol. 5677,pp169-176,2005

[2]M. Monoi, et al, SPIE Vol.7249 pp72490I-1-9, 2009

(a) All pixel readout mode



(b) 4-mix mode

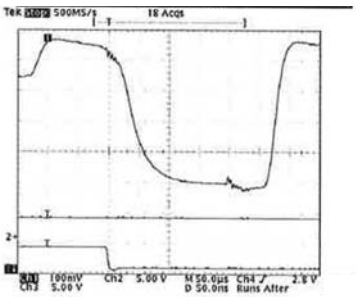


Fig.9 Output waveform

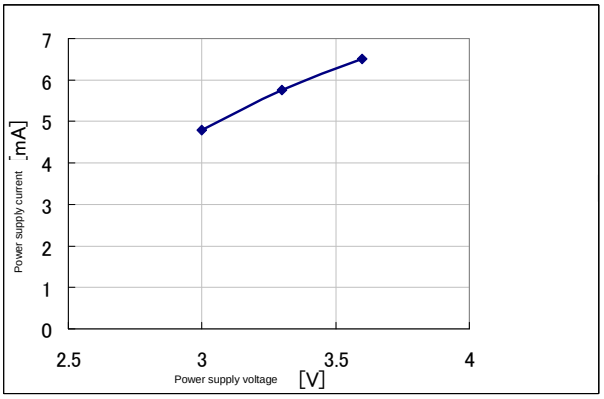


Fig.10 Power supply current

		1200dpi linear image sensor	
		CCD-CMOS combined	CCD
Power supply voltage		3. 3V	5V
Input pulse voltage		3. 3V	3. 3V
pixel number		688	688
pixel pitch		21. 16μm	21. 16μm
saturation voltage		1. 6V	2V
input capacitance		**CK1:11. 4pF** **CK2:12. 9pF**	CK1, 2:150pF
power dissipation		**16. 5mW**	37mW
responsivity		150V/lx・sec	157V/lx・sec
random noise		1. 1mV	1. 46mV
dark signal(10msec,25C)		2. 5mV	2. 4mV
die width		0. 23mm	0. 3mm
signal mix mode	clock frequency	(=1)	4times of left
1200⇒300dpi	random noise	1. 1mV	1. 46mV

Table.1 Characteristics of CCD-CMOS combined sensor, comparing with CCD sensor

		CCD	CMOS	**CCD-CMOS combined**
Readout noise		excellent	excellent	**excellent**
Power dissipation	Shift register	No good	excellent	**excellent**
	Output circuit	good	excellent	**excellent**
Integration simultanous		excellent	No good	**excellent**
signal mixing	Readout noise	excellent	No good	**excellent**
	Power dissipation	No good	excellent	**excellent**
Readout speed		excellent	good	**good**
Die size		good	good	**excellent**

Table.2 Comparison table with CCD, CMOS and CCD/CMOS combined sensor