P27 An Integration Time Prediction Based Algorithm for Wide Dynamic Range 3D-Stacked Image Sensors

Adi Xhakoni[1], David San Segundo Bello[2], Koen De Munck[2], Padmakumar Ramachandra Rao[2], Piet De Moor[2], Georges Gielen[1]
[1]K.U.Leuven, Dept. Elektrotechniek ESAT- MICAS
Kasteelpark Arenberg 10, B-3001 LEUVEN, Belgium
[2]IMEC, Kapeldreef 75 - B-3001 Leuven, Belgium
Tel. : +32 16 328618, e-mail: Adi.Xhakoni@esat.kuleuven.be

***Abstract*—We propose a wide dynamic range (DR) enhancement algorithm based on two frame captures. The first capture is used to predict the best integration time for the second capture. This way the DR enhancement is obtained with small dips in the signal-to-noise ratio (SNR). Furthermore, only one analog-to-digital (AD) conversion is required if analog correlated double sampling (CDS) is used, allowing low power consumption without compromising the maximum integration time needed for low light detection. A 3D-stacked system implementation of the algorithm is proposed and implementation issues are discussed.**

***Index Terms*—Wide dynamic range, 3D integration, global shutter**

I. INTRODUCTION

Due to their ability to integrate several functions in a single chip, CMOS image sensors are finding more and more applications in niche areas such as automotive, surveillance, smart traffic control etc. One of the most important figures of merit in image sensors is the dynamic range (DR). It is defined as the ratio of the brightest point of an image to the darkest point of the same image and it shows the ability of the detector to capture highlights and shadows in the same frame. Several methods are used to increase the dynamic range, with some of the most widely used being logarithmic pixel response, lateral overflow integration capacitor (LOFIC) and multiple captures. The logarithmic pixel operation allows simple pixel architecture and can obtain very high DR [1]. However, large noise at low light and image lag are clear disadvantages, mainly resulting from operating in the sub-threshold region of MOS transistors, where the diffusion current is dominant. Furthermore, variations in the fabrication process parameters may play an important role in the fixed pattern noise. The LOFIC method collects the charges generated by high luminance in an extra capacitor. This technique introduces a signal-to-noise ratio (SNR) dip at the switching point between the high conversion gain of the floating diffusion node (FD) and the low conversion gain of the LOFIC. This degrades the performance of the sensor once the required DR becomes high (more than 100dB) [2] [3]. The multiple capture technique allows wide dynamic range imaging by capturing images using different integration times and choosing the value closest to saturation [1]. However, this technique requires a large total frame acquisition time (T_{frame}) as shown in equation (1):

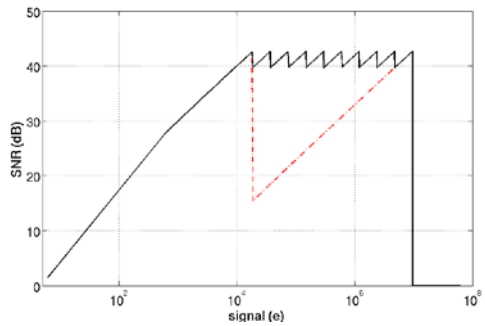

Figure 1: SNR characteristics of an image sensor implementing a dual capture (red line) and one implementing ten captures (black line)

$$T_{frame} = \sum_{i=1}^{n} T_{int}(i) + n(T_{AD} + T_{ro}) \qquad (1)$$

where n represents the number of captures needed for a certain DR, $T_{int}(i)$ the integration time of capture "i", T_{AD} the analog to digital conversion time and T_{ro} the pixel readout time. Furthermore, the multiple AD conversions needed per pixel (at least one for each capture) and the image processing required to reconstruct the final image [4] increase the overall power consumption.

To reduce T_{frame} in equation (1), a dual capture technique could be used. This method has a dynamic range enhancement given by equation below (same as the one with more captures), but with an SNR dip shown in equation (3):

$$DR_{ext} = 20\log_{10}\frac{T_{\max}}{T_{\min}} \qquad (2)$$

$$SNR_{dip} = 10\log_{10}\frac{T_{\max}}{T_{\min}} \qquad (3)$$

where T_{max} represents the long capture time and T_{min} the short one. *Figure 1* shows a comparison between two multiple capture techniques, one with dual capture (red, dashed line) and one with 10 captures (black line) where each capture time is twice the previous one. The large SNR dip shown by the dual capture would compromise the picture quality at mid-light levels. It follows that the extension of the DR with a dual capture technique depends on the maximum SNR dip allowed by the

specific application. We will present here a method which overcomes the SNR dip problem posed by the traditional dual capture technique.

II. IMPLEMENTATION

This section is organised as follows. Paragraph A introduces the algorithm for dynamic range extension while paragraph B shows a possible implementation of the algorithm using a 3D-IC stacking technology. In order to maintain small pixel pitch, some processing elements are combined at a group-of-pixels level. This requires a fast communication between each pixel and its corresponding group-of-pixels level processing in order to ensure high frame rate. Paragraph C discusses this issue and proposes a solution. Another important issue of the algorithm is the wrong prediction of the best integration time, and it is discussed in paragraph D, where a method to avoid pixel saturation is proposed.

A. WDR algorithm

This paper proposes a method which predicts the optimum integration time of each pixel with only two captures. The method works as follows. In order to limit processing simplicity and reduce SNR dips (see *Figure 1*), the total integration time is divided into sub-integration times $T_{int}(i)$ where each $T_{int}(i)$ is chosen according to equation (4):

$$T_{\text{int}}(i) = T_{\max} \cdot \left(\frac{1}{2}\right)^{n-i} \tag{4}$$

with T_{max} representing the maximum integration time of the frame and "n" the number of captures needed for a certain DR enhancement. According to equation (2), "n-1" is also the number of bits encoding the DR extension.

Figure 2 shows the flowchart representation of the algorithm. A first capture with integration time $T_{int}(1)$ (the shortest one) is used in order to predict the optimum value for the second integration time. The prediction is based on the comparison of the voltage read by the first capture, V_{c1}, with the reference value $V_t(i)$ obtained as shown in equation (5):

$$Vt(i) = V_{sat} \cdot \left(\frac{1}{2}\right)^{i} \tag{5}$$

where V_{sat} represents the saturation voltage of the pixel. During the second capture, before each $T_{int}(i)$, V_{c1} is compared to $V_t(i)$. In case Vc1 is higher than $V_t(i)$, the transmission gate of a pinned photodiode can be closed hence reading the pixel at integration time $T_{int}(i)$. In that case, the voltage read is stored in a sample and hold (S&H) capacitor, a mantissa bit is stored into a digital memory in order to perform a floating point DR extension [5] and a "veto" signal is sent back to the pixel to avoid further integrations within the same frame. After T_{max} all signals stored at the pixel S&H capacitors are read out and digitized.

Figure 3 presents three examples of three pixels with different luminances ("A","B" and "C"). The figure shows the voltage at the pixel resulting from the first capture with integration time $T_{int}(1)$ (bold and thick) and the predicted voltage with the optimum integration time which maximizes the DR (dashed line). Pixel "A" shows a first capture voltage value above $V_t(1)$ hence the optimum integration time for "A" is $T_{int}(1)$. In the case of B the voltage is below $V_t(1)$ but above V_{tmax} hence the optimum integration time for pixel "B" is $T_{int}(2)$.

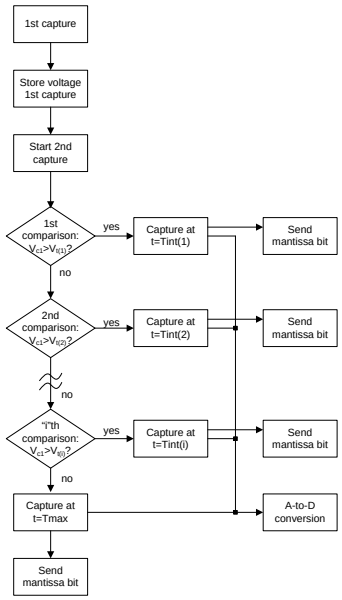

Figure 2: Flowchart of the algorithm

Pixel "C" presents a voltage lower than V_{tmax} at $T_{int}(1)$ hence the optimum integration time for "C" is the longest one, T_{max}.

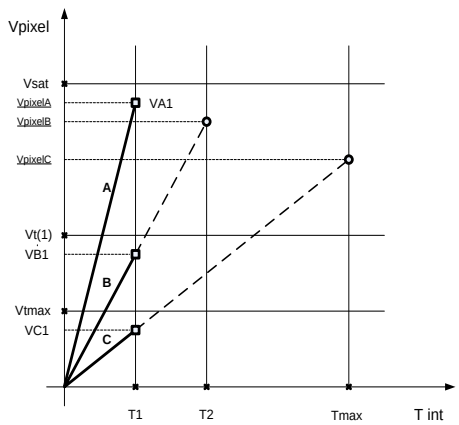

Figure 3: Three examples of pixel integration time prediction

B. 3D-IC stacked system implementation

A 3D-IC stacked system implementation of the algorithm is being built, in order to exploit all the benefits in terms of speed and low power consumption of such a packaging technology. Recent works ([6],[7]), have shown the design flexibility of using 3D-IC stacking in image sensors.

In an ideal implementation of the algorithm, each pixel would need to include a S&H capacitor to store the voltage read at the first capture, digital memory to store the "veto" signal [8] and the mantissa bits, digital gates to activate the pixel switches according to the "veto" value and a comparator to perform the comparison of the voltage read at the first capture with the reference values. If Correlated Double Sampling (CDS) is required, two S&H capacitors are needed, and the pixel can operate in a

true global shutter mode[9]. However, in order to keep a relatively small pixel pitch, some of the elements such as the comparator and the mantissa bits memory do not need to reside within the pixel, adding a tradeoff between processing speed and pixel size. For example, in a conventional monolithic sensor, the comparator could be shared by all the pixels in one column, but this would limit the frame rate, especially in case of high resolution arrays. In a 3D-IC stacked implementation, the comparator can be shared by an arbitrary group of pixels.

Figure 4 shows conceptually the system. It consists of three layers or tiers. The upper layer (tier 0), consists of the photodetector elements (e.g. pinned photodiodes). This first layer is connected to an analog readout and storage layer (tier 1) via bump bonds pixel by pixel. Each photodiode of the previous layer is connected to its own processing cell, excluding the comparator and the mantissa's digital memory. The comparator is shared by a group of pixels in this layer, while the mantissa bits are sent to the next layer. Through-silicon vias (TSVs) and bumps connect tier 1 to the last layer (tier 2). Tier 2 includes analog to digital converters (ADCs) and memory banks to allow digital frame and mantissa bits storage. Each ADC at tier 2 is shared by a group of pixels, ideally the same shared by the comparator. In both ADC and comparator pixel grouping, the size of the grouping directly influences the frame rate and the dynamic range hence small grouping is desired; however, this requires small pitch TSVs and it increases the pixel size.

A very interesting feature of working with groups of pixels is the theoretical possibility to maintain a constant frame rate while increasing the resolution if the grouping of pixels remains constant. This is valid provided that the interface to send the data off-chip can handle the increase in pixels/data rate. This is not the case when using column level processing: if the resolution is increased, also the number of pixels to be read by the same column level processing increases, limiting the readout speed.

Another benefit of 3D-stacking is the possibility to choose the best technology for each layer according to the functionality leading to possible cost saving and increased performance. In an ideal implementation, tier 0 would use a technology optimized for light detection (e.g. CIS), while tier1 would use one for high analog performance and tier 2 a deep submicron technology.

C. Select switch redistribution

In order to allow an efficient implementation of the algorithm without excessively compromising the frame rate, a fast communication is required between each pixel and its corresponding comparator. Common monolithic pixel arrays with row select (RS) switches sharing the same column bus (*Figure 5*) have high bus capacitance[10], reducing considerably the minimum integration time allowed by the algorithm. This is more evident when high resolution pixel array is used. Here we propose a new pixel select switch redistribution which decreases the load capacitance due to parallel switches from $N \cdot C_{sw}$ of a common monolithic sensor to $2 \cdot C_{sw} \cdot \sqrt{N}$ where N is the number of switches and C_{sw} the switch capacitance.

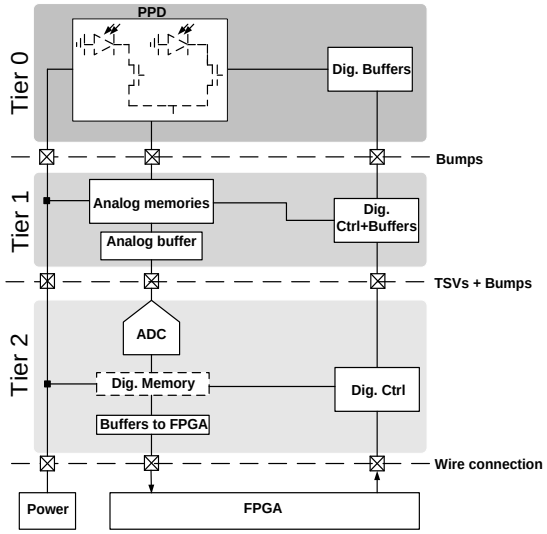

Figure 4: 3D-stacked architecture used to implement the algorithm

The implementation is depicted in *Figure 6*. The N switches of a single column of a monolithic implementation are spread into $\sqrt{N} \cdot \sqrt{N}$ pixels in a 3D-stacked implementation. A row switch is added at the end of the column allowing a smart column-row pixel selection type. Each pixel output will see a capacitance of $\sqrt{N}$ column select switches capacitance + $\sqrt{N}$ row select switches capacitance. All switches can be minimum sized transistors.

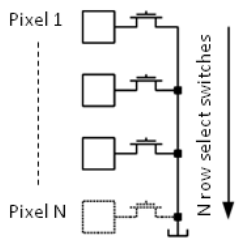

Figure 5: Row select swithes sharing column bus in a common monolitic pixel array.

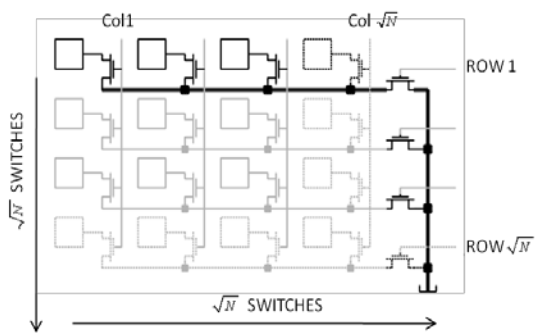

Figure 6: Reduction of load capacitance by adding row select switches at the end of the column.

D. *Offset effects in the prediction of the integration time*

If the voltage of the pixel at the time of comparison is very close to one of the reference values, the noise and offset at the input of the comparator can compromise the prediction of the best integration time. This would result, in the worst case, in the choice of a longer integration time than the optimal one, leading to pixel saturation.

Figure 7 depicts an example of a pixel with a measured voltage close to the lowest reference value and with an offset value which is half of the reference value. “A” represents the real value while “B” and “C” include the upper and lower offset levels respectively. The best integration time of the pixel is T_{int}(2). The upper offset level would cause the choice of a lower integration time, resulting in a slight reduction of SNR (up to ~3dB loss). “C” on the contrary can increase the predicted integration time, resulting in pixel saturation as shown by the red, dashed line. To solve this issue, the reference value should be adjusted according to the estimated offset value.

The reference values can be further decreased without decreasing the SNR considerably. For example a 50% reduction of the lowest reference value would result in a 3dB loss of the maximum SNR obtainable at that integration time. This feature is beneficial in the case of slight variability of light values during the integration period.

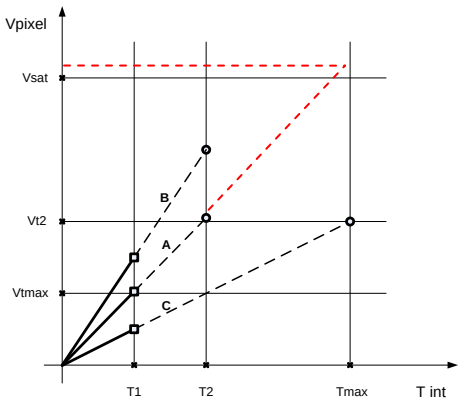

Figure 7: Effect of the noise in the prediction of the best integration time.

III. Conclusions

An algorithm for dynamic range extension based on a dual capture method is proposed. The first capture predicts the best integration time for the second one. With only 2 integrations, a maximum theoretical DR of $2 \cdot DR_{(0)}$ dB (with $DR_{(0)}$ being the intrinsic dynamic range of the sensor) is obtained with SNR dips of only 3dB. Another advantage of the method is that the integration time for low light detection is not compromised since $T_{frame} \sim T_{max}$ if the first integration time is chosen to be very small compared to the maximum integration time. Moreover, only the second capture is digitized allowing power reduction and a higher frame rate compared to conventional multiple capture techniques.

The proposed 3D-stacked implementation of the algorithm allows high speed and low power consumption. Issues such as effects of noise and offset in the prediction of the best integration time and pixel readout speed are solved by readjusting the reference values and applying smart pixel select switch redistribution respectively.

IV. References

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