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# Accurate capacitance and RC extraction software tool for pixel, sensor, and precision analog designs

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## Abstract

This paper presents a new CAD tool – F3D – for accurate 3D capacitance and distributed RC model extraction for image sensor designs. F3D overcomes limitations of existing parasitic extraction tools and field solvers, and enables a predictive accurate capacitance extraction and distributed RC model generation, automated identification of all relevant capacitive coupling components, including long-range coupling, and detecting even small (down to 0.01% or better) capacitance mismatch caused by layout effects.

## Introduction

Image sensor designs include many structures and circuits that are very sensitive to capacitive and resistive effects caused by metal interconnects and devices. These effects can be unintentional, i.e. parasitic – such as floating diffusion (FD) node capacitance being impacted by parasitic capacitance between metal/contact/poly structures, or delays along clock or signal nets caused by distributed RC effects, or intentional – such as capacitance of MIM or MOM structures used in sample and hold circuits, ADCs, and other circuits. Extraction (calculation) of capacitances and resistances of metal interconnects can be performed using software tools that fall into two categories: 1. popular parasitic extraction tools used in IC design flow, and 2. field solvers. The parasitic extraction tools (group 1), based on a pattern-matching method, are fast but not accurate enough and their accuracy cannot be controlled. Field solvers (group 2) can provide an acceptable accuracy, but their capacity (the size of the design) is severely limited by the constraints of the 3D mesh required for calculations. A new class of field solvers, based on random walk method [1,2], capable to extract large designs with high precision and accuracy appeared recently.

## F3D – capacitance and RC extraction tool based on random walk method

F3D is a rigorous field solver based on stochastic random walk method (see Figures 1 and 2, and references 1 and 2), enabling capacitance extraction of complex three-dimensional large-area structures – such as pixels, arrays, and precision analog circuits (ADC, electrostatic shields, etc.). Unique features of the tool – user-definable capacitance calculation accuracy, mesh-less simulation method free from boundary condition and meshing artifacts, integration with standard physical verification flows, SPICE-compatible output (DSPF file), and ease of use – make it superior to existing popular parasitic extraction and field solver software tools [3]. Application of F3D for calculation of floating diffusion (FD, or sense node) capacitance with varying metal layouts shows an excellent agreement with the measurement data.

## Floating diffusion (sense node) capacitance problem

FD capacitance determines the pixel conversion gain, and it should be designed to a specific target value. Capacitance of small-size pixels is dominated by the coupling capacitances between the FD metal net and neighboring metals (Fig.3). Capacitance tuning can be easily achieved through metal layout optimization – provided that the capacitance extraction tool is reliable and accurate. Fig. 4 illustrates an excellent agreement between simulation and measurement results. F3D predicts the capacitance trend for varying metal layouts with absolute accuracy, and the total FD capacitance values with one-point calibration (F3D does not simulate semiconductor electrostatics and thus does not extract p-n junction and other non-linear capacitive semiconductor effects).

## Application of F3D for ultra-high precision extraction

At the same time, F3D can be used as a general-purpose parasitic extraction tool providing guaranteed accuracy on large designs. One of breakthrough applications is super-high accuracy extraction of nets with nominally matched or weighted capacitances, such as in capacitor bank of SAR ADCs. Due to a close proximity of column ADCs (caused by pixel pitch constraint), parasitic coupling from the capacitor plates to the “outside world” violates prefect capacitance weighting and leads to integral and differential nonlinearities (INL and DNL) and loss of ADC resolution. F3D enables to detect capacitance mismatch as low as 0.01%, to identify the root causes of the mismatch that are related to the layout, and thus to achieve a more reliable and higher performance designs from first silicon. In many situations, what is important is not the absolute or relative accuracy of capacitance extraction, but an identification of the presence of small, long-range capacitive coupling critical for many designs. This problem is common in aggressor-victim nets electrostatic interaction that may have very long range, may be very small (as compared to the total net capacitances) and may not be easily identifiable by a layout inspection due to a huge design size. Random walks performed during capacitance extraction by F3D tool help to automatically identify and report all significant capacitance coupling components.

## Passive device capacitance extraction

Active and passive devices used in ICs are described by compact (SPCIE) models and should be excluded (or “blocked”) from parasitic extraction (thus, blocking in parasitic extraction is a process inverse to device de-embedding in device compact model extraction from measurement data). However, the “boundary” between the devices and interconnects is often blurred, or not well defined, especially when device are not perfectly shielded from the environment. In particular, MIM and MOM capacitors in image sensors often have small size or width. Therefore, their capacitance is strongly affected by the surrounding interconnects and other devices, which cannot be accounted by their simplistic compact models describing only area and periphery capacitance components. Instead, MIM and MOM capacitors can be treated as interconnects and simulated with F3D, to achieve higher accuracy for device and interconnects capacitance models, and for predictive post-layout circuit simulation.

## References


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2. A. Brambilla and P. Maffezzoni, “A statistical algorithm for 3-D capacitance extraction”, IEEE Microwave and Guided Wave Letters, v. 10. no. 8, pp. 304-306.
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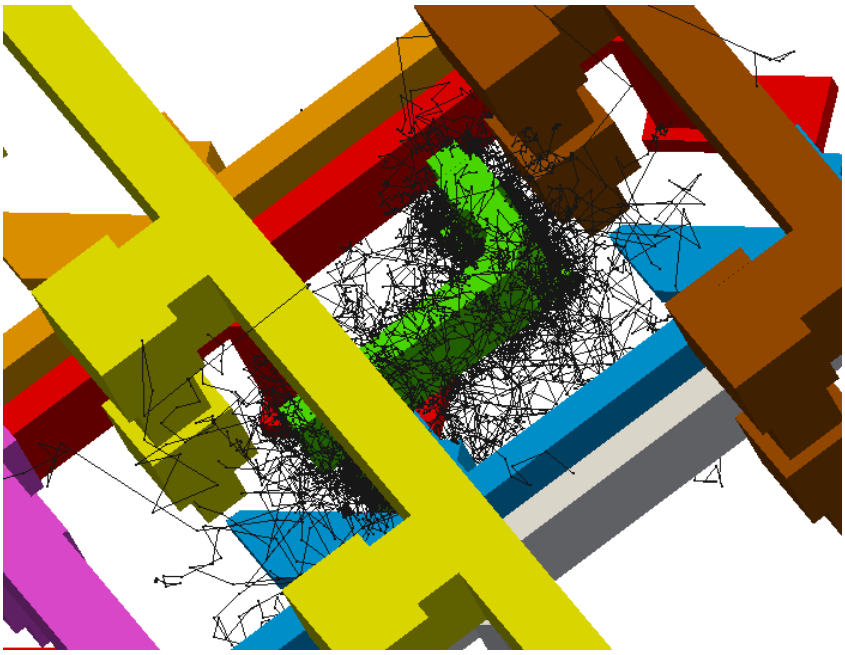

4.

Fig.1. Illustration of the floating random walk method as applied for capacitance extraction problem. A large number of random walks (consisting of a series of hops) are started from the Gaussian surface of a net to get a statistical estimate of the capacitance coupling between this net and all other nets. Probabilities of hops are determined by Green's functions of the electrostatic potential. Random walks automatically find all the nets that are capacitively coupled to the net of interest.

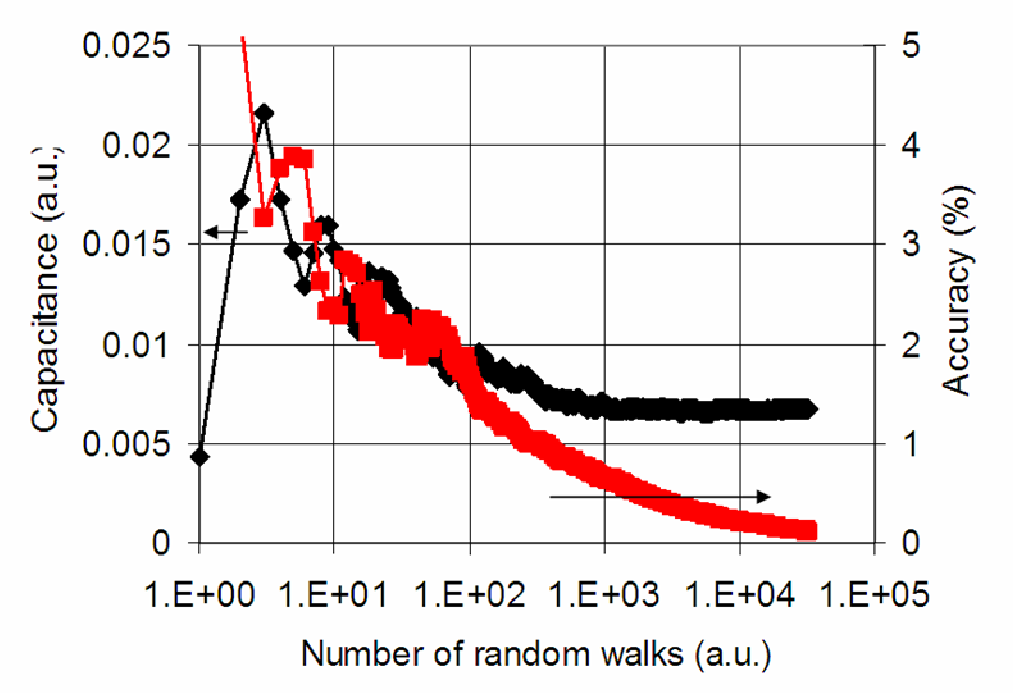


Fig.2. Illustration of random walk method convergence for calculated capacitance and reduction of statistical error of capacitance value with increase of the number of random walks.

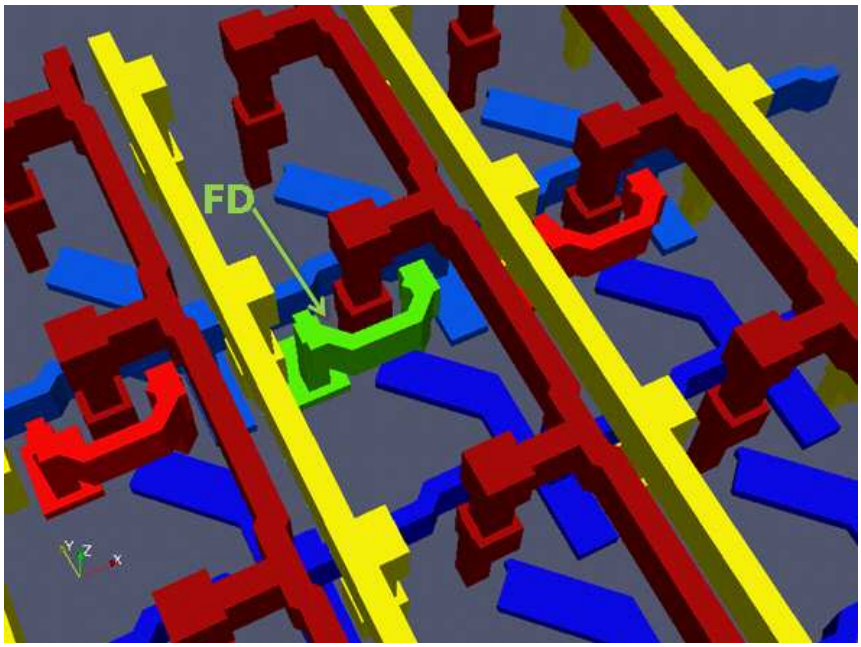


Fig.3. Example layout showing couplings between FD and neighboring metals.

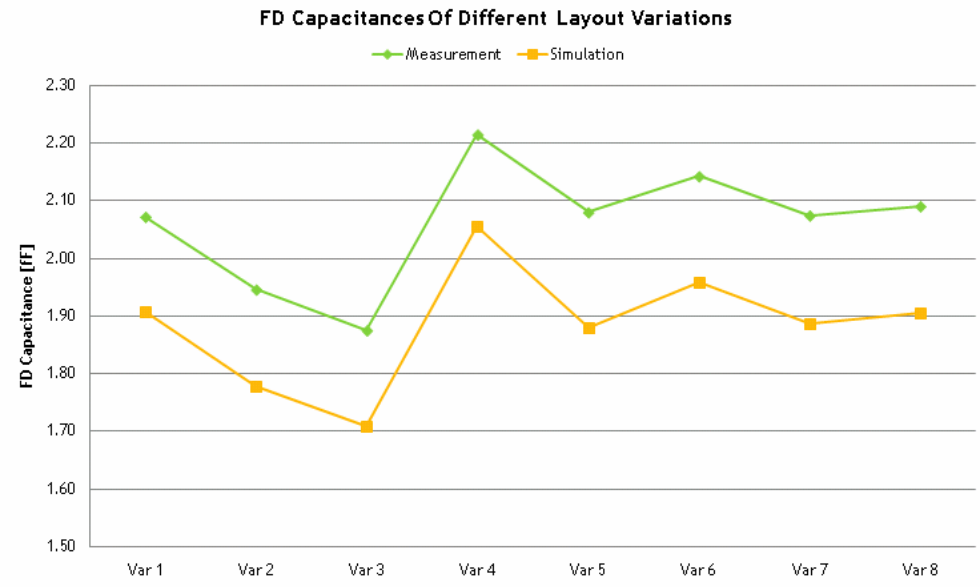


Fig.4. Comparison between measurement and simulation results of FD capacitance.