Backside Illumination Technology
For SOI-CMOS Image Sensors

Bedabrata Pain
Edict Inc
bpain@sbcglobal.net
310-666-6749

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PROBLEMS of SMALL PIXEL

PIXEL SCALING TRENDS

Continuous Technology “Breakthrough” Needed to Keep up with the Scaling Trend

Metric \( \frac{FW(e) \cdot Tech(\mu m)}{V_{dd}(V) \cdot Pitch(\mu m)} \)
ANGULAR RESPONSE

Numerical aperture

Stack-height + Obscuration
- Sensitivity loss
- Vignetting
- Color X-talk
- Spatial variation of x-talk
- Poor angle response

Telecentricity

DETECTIVE QE (MODIFIED)

Photons Noise+XT

Output

How well does it transfer power?

\[
dQE = \frac{SNR_{out}^2}{SNR_{in}^2} = \frac{QE^2(1-\alpha^2)\alpha^2}{QE(1-\alpha)+\alpha|N_\alpha|}
\]

\[
= QE \left[ \frac{(1-\alpha)^2}{(1-\alpha)+\frac{\alpha}{P} \frac{N_\alpha}{QE}} \right]
\]

[1, 2]

Increase QE (QE >= 100)
Reduce Noise (N_\alpha=0)
Eliminate X-talk (\alpha=0)
FRONT-SIDE ILD MODIFICATION

THINNER FRONT-END [3]

Cu Process

Metal 3
Metal 2
Metal 1
Silicon

20% Shrink

Micro Lens
Color Filter

Metal 3
Metal 2
Metal 1
Silicon

Process Complexities
Basic Problems remain

LIGHTPIPE APPROACH [4]

Photo-diode

gate 1.5 μm

Difficulties in material selection

BACK-ILLUMINATION
BACK-ILLUMINATION: A SOLUTION

- High Sensitivity and quantum efficiency
  100% fill-factor
- Excellent X-talk and Angular Response
  "Canyon" effect eliminated
  No obscuration
  Spurious reflections eliminated
- Efficient microlens and anti-reflection coating
  Planar surface
- Advanced pixel processing
  Dynamic range expansion
  Global shutter
  Gain ranging
  Low noise
- Compatibility with next generation dielectrics and metals

CROSS-SECTION

- Collection much closer to microlens
- No Obscuration
- Supports larger numerical aperture
BACK TO MAXWELL

Plenty of optical energy leakage due to pixel dimension, wave-effects, CFA

FDTD simulation of energy coupling

OPTICAL ADVANTAGE

Optical Coupling into Silicon for 1.75 μm pixel

Front Illumination (TE/TM)  Back Illumination (TE/TM)

Almost 3x improvement at F 2.0
QE & OPTICAL CROSS-TALK

- QE goes down and Cross-talk goes up
- QE loss due energy spread via E-M field propagation
- Front-side QE also limited by imperfect AR coating

BACK-TINNING ISSUES

Manufacturable + Wafer-level Processing + Good device performance

- Accurately thinning 700 µm substrate with <50 Å surface roughness
  - Appropriate etch-stop
- Backside passivation
  - Hold exposed surface in accumulation
- Device support (during and after thinning)
  - Attachment of support wafers – must allow post-processing
- Packaging
  - Where do pads come out from? Wire-bond or CSP?
- AR coating, Color, Microlens
  - Alignment key
  - Stack issues
- Diffusion Cross-talk Control
  - Field-shaping implants
  - Back-surface gradients
PASSIVATION PROBLEM:
- Exposed Si-SiO₂ interface quality is poor
  - high trap density, potential pocket due to band-bending
  - loss of blue QE and high dark current

BACKSIDE TREATMENT
- Implant + RTA Anneal
  - Cannot be used due to the presence of metals
- Implant + Laser Anneal [6, 7]
  - PRNU, Dark current
- Delta-doping: few monolayers of boron added by MBE to the back surface [8]
  - Excellent results, but non-standard process
- Flash gate: deposited oxide + UV flooding [9, 10]
  - Outgassing, Long-term stability
  - Non-desirable metal; AR coating issues
- Back-gate: deposited oxide + ITO gate
  - Process Control; AR coating issues
FABRICATION STEPS

SOI TO THE RESCUE

Thin silicon layer: 200 nm
BOX: 200 nm

Small Pixels [13]

CMOS readout/ADC
Metal interconnects
Pixels in handle wafer

Thick Silicon Substrate

NIR enhanced Imager [12]

Thick silicon layer: 2-10 µm
BOX

Pixels

Metal interconnects
SOI IMAGER FABRICATION

- SOI wafer with thick device layer (~ 2-10 µm)
- Imager-compatible bulk-CMOS process

Starting Wafer → Bulk-CMOS process → Support wafer attachment → Wafer thinning → Backside coating → Pad Opening

- Provides mechanical support
- Bonding process/material must be back-end compatible
THINNING

- Wafer-level thinning
- Natural high-selectivity (Si-SiO₂) etch-stop

PASSIVATION

- Buried oxide made by thermal oxidation
- Pre-implanted region for passivation
- Self-passivation: surface never exposed

Chemical Etch

- Hot KOH/TMAH wet-etch
- RIE with SF₆
- XeF₂ vapor-phase

<table>
<thead>
<tr>
<th></th>
<th>KOH</th>
<th>SF₆</th>
<th>XeF₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local</td>
<td>&lt;20A</td>
<td>&lt;500A</td>
<td>&lt;20A</td>
</tr>
<tr>
<td>Global</td>
<td>&lt;200A</td>
<td>3000A</td>
<td>&lt;40</td>
</tr>
</tbody>
</table>

BACK-to-FRONT ALIGNMENT

Exposed metal holds alignment keys
**PAD OPENING**

- Deposited oxide
- Deposited oxide/nitride
- Planarized oxide
- Glass wafer

**THE CROSS-SECTION**

- Handle Silicon
- BOX
- Device Silicon: 3.3 µm
- ILD
- M0
- p-Si
- p-substrate (50 Ω-cm)
- Deposited oxide
- Deposited oxide/nitride
- Planarized oxide
- Glass wafer
- Cross-section after thinning

- p-Substrate (20 Ω-cm)
- Integrated SiO2 (ILD)
- Implanted wells (devices)
- Metal trace (0.7 µm thick)
- Planarized oxide
- Deposited oxide/nitride
- Deposited oxide
ALTERNATE INTEGRATION SCHEME

- Through silicon via is formed at the first metalization step
- Liner oxide for isolation
- Serves as alignment key for CFA/ML

Deep silicon via formation

Support Wafer + Thinning

Final Cross-section

[17, 18]
POSSIBLE EVOLUTION

1\textsuperscript{st} Generation
Through Silicon Contacts for wirebonds
Pixel optimization

2\textsuperscript{nd} Generation
Higher Dynamic Range – In-pixel Cap
Better Z-height - WLCSP

3\textsuperscript{rd} Generation
Only pixel in wafer – best performance
SOC integration

PERFORMANCE
COLOR BIS IMAGER

Back-illuminated 1.75 µm Color Picture

PERFORMANCE IMPROVEMENT

Median luminance = 3 lux

Median luminance = 690 lux for D65

↑ 2.5x increase in Sensitivity for 2.2 µm pixel
↑ Dark current & Full-well about the same
↑ Angular response improves by 5x
↓ Electrical cross-talk worse
**QUANTUM EFFICIENCY**

- Surface Boron is an effective tool to improve QE
- Blue QE affected by boron content at the surface
- For color Imager: 20% loss going through CFA and OCL

**WELL BEHAVED DARK CURRENT**

- Front Illuminated
- Nitride cover
- Back surface Boron
- Nitride + H$_2$ anneal
- Dark Current (e/sec)

<table>
<thead>
<tr>
<th></th>
<th>Front Illuminated</th>
<th>Nitride cover</th>
<th>53</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum</td>
<td>None</td>
<td>None</td>
<td>8000</td>
</tr>
<tr>
<td>Small</td>
<td>None</td>
<td>Yes</td>
<td>419</td>
</tr>
<tr>
<td>Medium</td>
<td>Yes</td>
<td>Yes</td>
<td>133</td>
</tr>
<tr>
<td>High</td>
<td>Yes</td>
<td>Yes</td>
<td>57</td>
</tr>
</tbody>
</table>

[14]
ANGULAR RESPONSE

Slight increase in relative angular response is due to optical path difference

BACK FIELD

- Simulated Nominal Back doping gradient and electric field
- Back-field drives minority carriers towards front
- Back-field suppresses Cross-talk
- Proper doping gradient is extremely important

Doping Trade-offs
RTS NOISE REDUCTION

- Source follower as the main source of RTS
- Both modal noise and noise spread is reduced by length increase

\[ C_{SH} = 1.5 \, \text{pF}; \quad G_{cp} \approx 45 \, \text{\mu V/e}; \quad I_{bias} = 3 \, \text{\mu A} \]

MANUFACTURABILITY ISSUES
SUPPORT WAFER BONDING

Acoustic micrograph of low-temperature oxide-oxide bonded support wafer (courtesy Ziptronix, Inc.): No voids

Passes die-level thermo-mechanical tests (thermal shocks and temperature cycles)

Alternate schemes? [17]

“PEEL OFF”

DELAMINATION

EDGE EXCLUSION

Sawing Process optimization to prevent delamination

Optimization of bonding and grinding process to eliminate edge-cracking during subsequent processing
THE THREE THINGS ...

- Back illumination
- Front illumination

Electrical Cross-talk
- Separated generation and collection area
- Back surface field
- Deeper Junction

QE
- Integration of AR stack on the BOX

Dark Current
- Back surface passivation with integrated AR stack

AR STACK OPTIMIZATION

- Excellent AR stack can be achieved with SiN/SiO layers
- Need to ensure that angular response is acceptable
- BOX not the ideal-choice for 1st AR layer
DARK CURRENT with AR STACK

BOX etching does not increase dark current, if done right!

CROSS-TALK

• Boron needed to passivate interface states
• Boron gradient needs to be optimized
• Boron segregation is the source of problems
• N-type substrate is preferable
CROSS-TALK TRADE-OFF

- Diode doping profile engineering for deeper field penetration
- Optimize silicon thickness
- "Clean-up" back surface: Boron segregation could be a problem
- Modify CFA?
- Modify microlenses
- Optimize AR stack

MOVING FORWARD (in lieu of conclusion)

Cost - how low can you go?
Special SOI wafer needed?
Will SOI wafer become cheaper and have shorter turn-around time?
Where are the yield and reliability "gotchas"?

Performance
SOI wafer quality? Will lack of gettering be an issue?

Alternate Support Wafer Attachment
Need for an alternative to LT-bonding? Alternate support materials?

Appropriate Optical Stack
What materials for AR stack?
Alternate CFA?

Improving Cross-talk
Boron segregation - N-type material?
Alternate diode profiles and barrier implants? Deep trenches?
Alternate dielectric for improved passivation? ITO?

Packaging
Chip-on-board (COB) or Chip-scale-packaging (CSP) or wafer scale (WSP)?
REFERENCES