

12Mpixel snapshot shutter CMOS image sensor with 5.5um pixels operating @33fps with high shutter efficiency

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Abstract This paper presents a 12Mpixel pipelined snapshot shutter CMOS image sensor with high shutter efficiency. The sensor is a stitched design of 5.8cm wide and 1cm tall. The pixel array features 10,000 x 1200, 5.5um square pixels with micro lenses and color filters. Both a monochrome and color sensor are processed on the same die with the pixel arrays only 700um distance from each other. The sensor operates at 33fps in full frame readout with 8 analog outputs each operating at 50 Msamples/s. Key parameters for this imager are high shutter efficiency (>86dB), low crosstalk (MTF>60%) and a dynamic range of 62dB. The sensor is designed in a standard 0.18um CMOS process and consumes less then 0.5W in full operating mode at 33fps.

1. Introduction

This 12Mpixel snapshot shutter sensor with high shutter efficiency is primary designed for earth observation applications in assignment for VITO (Flemish Institute for Technological Research). The pixel array contains 10,000 x 1,200, 5.5um square pixels with microlenses and color filters resulting in a die size of approximately 5.8cm x 1cm after stitching. It is able to operate at 33fps in full frame readout with 8 analog outputs each operating at 50 Msamples/s. A simplified block diagram of the sensor is presented in figure 1.

Both the monochrome and colour sensor are processed on the same die as presented in figure 2. One advantage of such approach is that they are surface-aligned. It is possible to only dice one sensor (color or mono). This was enabled by adding a scribe line between the color and mono sensor regions.

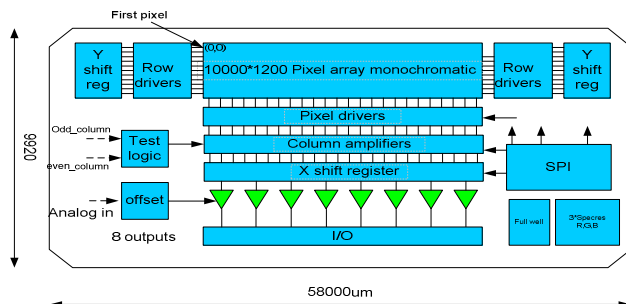


Figure 1: Block diagram of 1 sensor

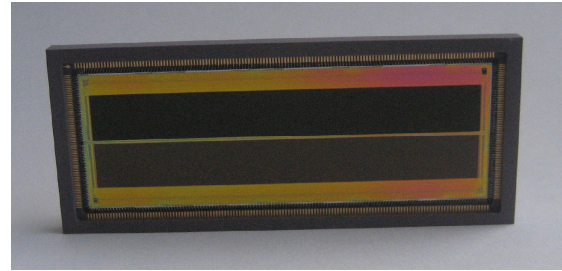


Figure 2: Mono and color sensor on 1 die inside package.

2. Sensor Architecture

The Imager consists of 3 different stitch blocks, 2 stitch blocks at the sides (only containing periphery circuits) and the pixel array which consists of 4 equal stitch blocks, each 13750um long with 2500 by 1200 pixels. Furthermore, every pixel array stitch block has an independent read out path including 2 output amplifiers each operating at 50Ms/s allowing the total sensor output data rate up to 0.4GSamples/sec (8 analog outputs).

The sensor consumes less then 0.5W at full speed operation and 0.1W in standby mode. This standby mode can be enabled by an external digital signal. By the use of this standby mode, one can decrease the power consumption dramatically when lower frame rates are allowed but fast readout speed needs to be maintained.

A fast readout speed can be required in a snapshot shutter sensor because every pixel contains a memory element which has a certain parasitic leakage. If the readout time is low, a gradient in the image might be observed. This is due to the fact that the last pixels need to hold their values longer in their memory element. This new custom sensor can readout the whole pixel array (12Mpixels) in less than 30ms, which means that the effect of any parasitic leakage will be small on the observed image.

3. Novel 6T pixel architecture

Due to a new pixel design, this sensor has low dark leakage of the memory elements (PSNL), low parasitic light sensitivity (PLS) while still maintaining a relative high FF(fill factor) and QE (Quantum efficiency) as well as a high MTF (Modular transfer function). The pixel schematic is presented in figure 3. As can be seen in the schematic, the memory capacitor consists of a transistor where that the signal is sampled on the poly-gate of the memory transistor which is properly biased to form a stable capacitor. A transistor is used because in most available 0.18 technologies, a poly to n+ capacitor is not possible (this would require an additional mask).

In previous 6T pixels, sampling occurred on the diffusion of the memory transistor while its poly gate was biased high to ensure a stable capacitor was formed for all possible sampled voltage levels. However, the disadvantage of sampling on the diffusion of this transistor is that the dark leakage (PSNL) and parasitic light sensitivity (PLS) will be relatively high.

In order to improve the PSNL and PLS, The choice was made to sample on the poly-gate of this transistor instead of the diffusion. The problem with this approach is that the minimum sampled value always needs to be higher than the threshold voltage (V_t) of this transistor in order that the transistor operates in strong inversion and maintains a good stable capacitance. To tackle this problem, a low V_t implant is used for the memory transistor as well as a relative high lower reset voltage (1.3V). By doing so, the sampled value on the memory transistor will always (even when the photodiode is saturated) be higher than its threshold voltage resulting in a good capacitor.

Another improvement compared to traditional 6T pixels is the way of precharging this memory capacitor. Traditionally, the precharge transistor's drain is connected to a ground substrate contact inside the pixel or a separate metal line connected to gnd in the sensor's periphery.

In this 5.5um pitch pixel, this would reduce the fill factor dramatically. Therefore, the source of the precharge transistor is connected to the output of an adjacent pixel as described in figure 4. This is possible because the precharging of the sample capacitors of the pixels is done during the frame overhead time (A possible pixel timing is presented in figure 6). In that time, there is no readout ongoing which means that the columns are connected to ground in order to precharge the pixels. The advantage of doing this compared to precharging to a ground substrate contact inside the pixel or additional metal line is 2 folded. Fill factor is increased and less drain source leakage is observed during readout. The gain in fill factor is quite dramatic because a common source for both the select transistor of the adjacent pixel and the precharge transistor of the current pixel is used as described in figure 5. By

doing this, no interconnect between the two transistors is required. The reduction in drain source leakage is due to the fact that during readout, the columns are on higher than zero voltage making the gate source voltage (V_{gs}) of the precharge transistors in the pixels negative which reduces it's leakage directly.

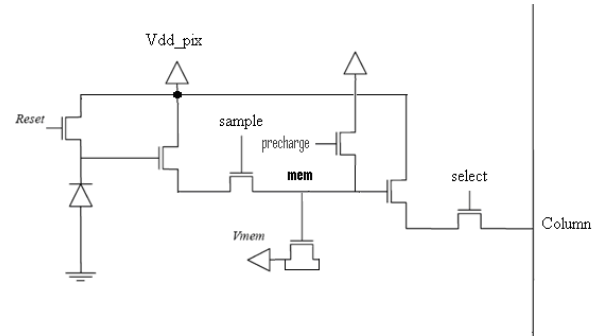


Figure 3 : Low PLS/PSNL high fill factor 6T pixel architecture.

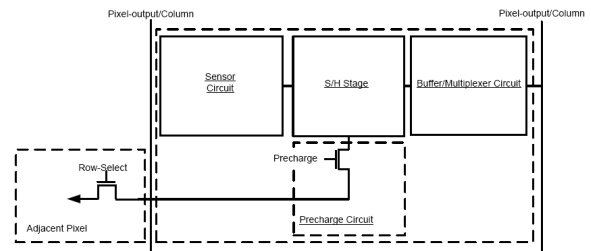


Figure 4: Simplified diagram on how the precharge transistor is connected to the output of an adjacent pixel.

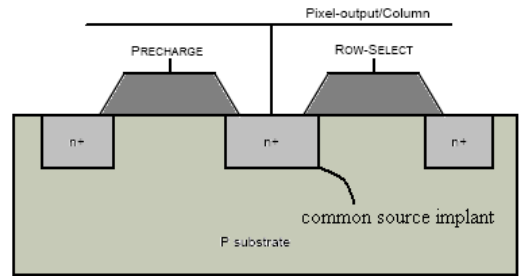


Figure 5: Simplified cross section of pixel area where the precharge and select transistor share a common source implant.

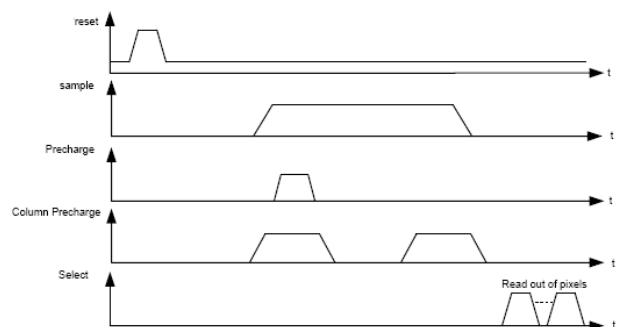


Figure 6: Example of a possible pixel timing.

4. Column structure for high speed bus driving and low column FPN.

The measured sensor's image quality sets new standards in its application area, not only due to the new pixel design but also due to a novel column structure and bus driving circuit. Due to this new read out method, the internal bus speed has increased, making single pixel kernels possible. This has the advantage that after-bus multiplexing isn't required anymore, improving the overall fixed pattern noise (FPN) of the sensor. The old traditional column structure as well as the new column structure have been implemented on this sensor to check the difference directly. As seen in the raw image shown in figure 12, column FPN is not noticeable when the new column structure is operational. Figure 13 presents the image when the traditional column structure is used. A comparison of figure 12 and figure 13 shows that the image quality has improved significantly, column FPN can't be observed by the naked eye and dynamic range has increased in the new developed column structure.

The new column structure uses a high gain amplifier with a double feedback path from the bus driving switch as described in figure 10. By this structure, the phase margin can be externally controlled by an analog DC voltage to optimise the settling time. This increases the bus driving speed significantly compared to traditional bus driving circuits.

Traditionally, the bus driving occurs as described in figure 7 and 8. This bus driving topology is in most cases speed limited by the resistance of the used switch (which connects the column amplifier to the multiplexer bus). The reason why this switch is the limiting factor is due to the fact that the switch W/L can not be made very large to improve the driving capability. This is because a lot of these switches connect to the same bus and an increase in W/L will increase the total bus capacitance. Therefore an optimal switch size exists to have the optimal resistance/bus capacitance for the highest speed and in most cases, its resistance is relatively high.

A possible solution would be to connect the feedback path at the bus instead of at the column amplifier output. This is described in figure 9. In that case, the amplifier will overdrive its output to compensate for the relative high switch resistance. The switch resistance seen from the bus will then be reduced by approximately a factor of the open loop gain of the column amplifier. The problem with this approach is that by doing this, an additional pole is introduced in the transfer function reducing the phase margin and possibly resulting in unstable operation. This is especially true when a high gain column amplifier is used.

However, there is a solution to still be able to compensate for the switch resistance and maintain stable operation when a high gain column amplifier is used. The trick is to

use a double feedback path from the bus driving switch (see figure 10, feedback path via transistors M2 and M3) in order to also provide the amplifier's output information (at the left of the switch M1) to its input so it can adjust itself faster which results in a more stable operation. The resistance ratio of both feedback paths will control the systems phase margin. An optimal ratio in resistance between both feedback paths exists to have the fastest possible settling. It must be noted that the layout of this bus driving topology needs to be done very carefully to match the transistors as good as possible between the columns to make it work properly over this long sensor.

A comparison between the simulated bus settling times for the new bus driving topology and the traditional bus driving topology is given in figure 11. Approximately a factor 2 in bus speed is gained by this double feedback bus architecture.

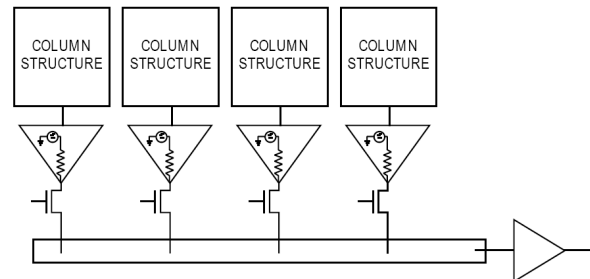


Figure 7: Simplified column to multiplexer bus connection diagram.

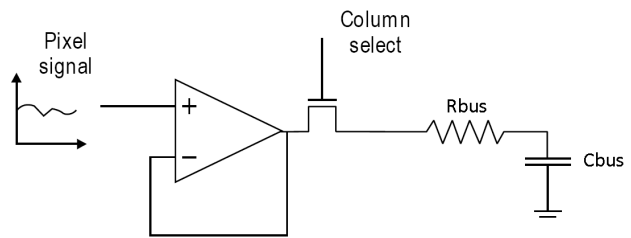


Figure 8: Traditional column to bus driving topology, switch impedance is in most cases the limiting factor for the maximum bus speed.

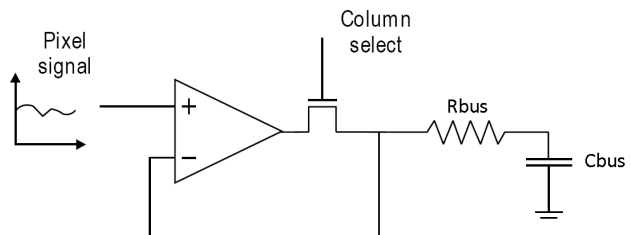


Figure 9: Feedback after bus driving switch reduces the driving impedance but can introduce unstable operation.

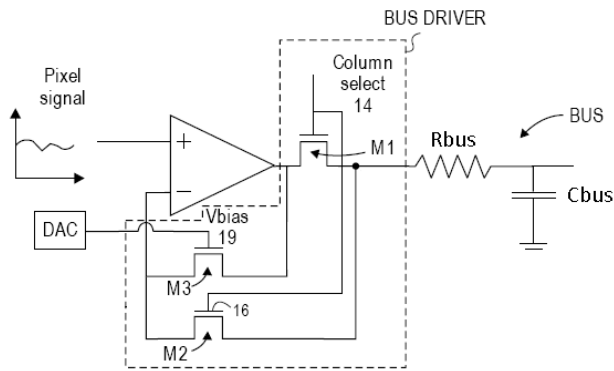


Figure 10: Double controlled feedback path from bus driving switch increases bus driving speed while maintaining stable operation.

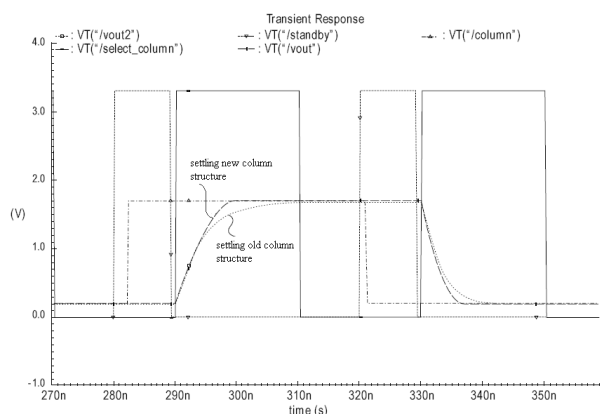


Figure 11: Improvement in settling time between new bus driving topology compared to traditional bus driving topology. (Simulation result)

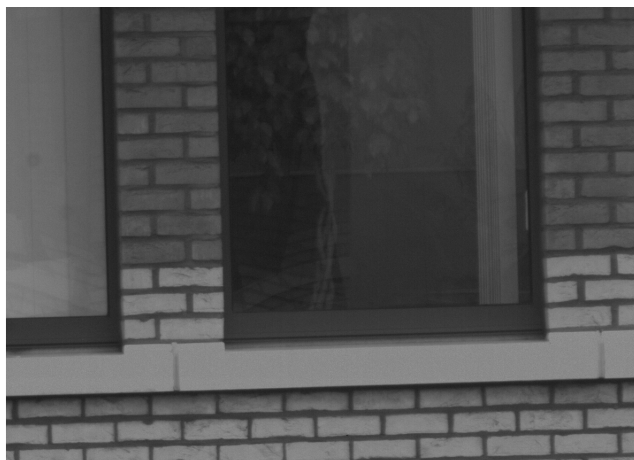


Figure 12: Part of the raw image with new column structure: No column FPN observed by naked eye.

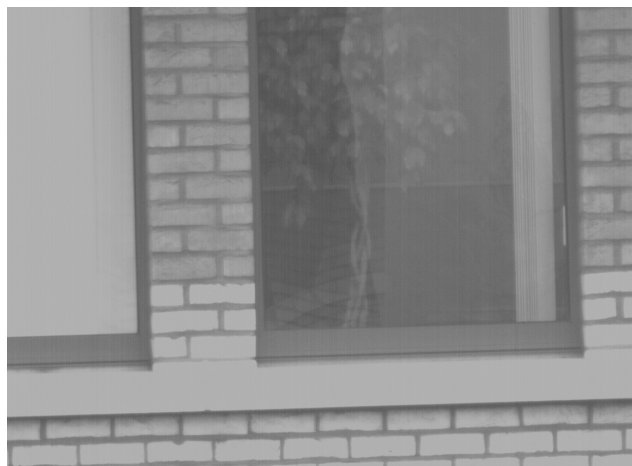


Figure 13: Part of the raw image with old column structure: column FPN is introduced as well as significant lower dynamic range.

4. Characterisation results

This pixel has measured PSNL and PLS values smaller than 5mV/sec and 1/30000 respectively. This is a huge improvement compared to similar snapshot pixels of this size (typically PSNL and PLS values were in the order of 30mV/sec and 1/1000 respectively). With this low storage node leakage and improved PLS, the readout time can be increased significantly without degrading the image quality.

Furthermore, the sensor/pixel has a total output swing larger than 1.2V and a full well charge exceeding 33000 e- in the linear region (<6% pk-pk). The dark read noise is approximately 1mV which yields in a dynamic range of 62dB with the possibility to go up to 90dB by using multiple slope operation. The measured optical/electrical crosstalk (expressed as MTF) of this 5.5um pixel is state-of-the art. This sensor has an MTF higher than 60% at Nyquist frequency in both X and Y directions while still having a fill factor of over 65%. This makes it possible to provide sharp images in low light conditions.

An overview of all the important specifications and measurements is listed in table 1.

Technology	0.18 μ m CMOS process
Die size	58mm*9.92mm
Packaged chip size	25.0 mm (H) x 29.0 mm (V)
Array size	10000 (H) x 1200 (V)
Frame rate	33 fps at full resolution
Shutter type	Pipelined snapshot shutter
Supply voltages	3.3V, 1.3V and 4V
Power consumption	<0.5W
Operating temperature	-40°C to 60°C
Color	Monochrome and Color (same die)
Pixel type	6T variant
Pixel size	5.5 μ m x 5.5 μ m
Peak QE	48% 550nm, with micro lenses
Conversion gain	35 μ V/e ⁻
Temporal dark noise	28 e ⁻
Pixel saturation charge	>35000 e ⁻
Dynamic range	62dB
SNR(shot noise limited)	>45dB
Dark current	6mV/s at 20°C
PRNU	1.6 % @ half saturation
FPN	30mV
Column FPN	<3mV
PLS	<1/30000
PSNL	<5mV/s
MTF @ 630nm @ Nyquist freq.	>60% in both X and Y directions
Data rate	50MHz input clock, 50Mbit/s data rate per channel 0.4Gpix/s aggregate pixel rate
Interface	8 Analog outputs
Package	Custom PGA

Table 1: key specifications and measurements.

References

1. Medusa - Monitoring Equipment and Devices for Unmanned Systems at high Altitude, <http://medusa.vgt.vito.be/>.

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5. Conclusion

A wide 12Mpixel CMOS sensor with a novel global shutter pixel exhibiting high shutter efficiency is presented in this paper. The applications for this sensor are very broad, from earth observation systems to high speed industrial vision as well as 2D bar code readers and wide area security camera systems.

6. Acknowledgements

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