Image Artifacts Caused by Pixel Bias Cells in CMOS Imagers targeted for mobile applications

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***Abstract*—The quality of an image produced by a CMOS image sensor is strongly linked to the quality of the pixel bias cells. However the voltage or current bias circuits and their effect on an image is rarely written about in the literature. This paper describes a number of artifacts seen if the bias cells are not properly designed.**

I. INTRODUCTION

State of the art CMOS image sensors are built around the pinned photo-diode pixel [1]. To properly bias the pixel and enable it to work properly, eight bias cells are typically required. These are Vtglo, Vtghi, Vrstlo, Vrsthi, Vrdlo , Vrdhi, Vrt and Icol and are shown in Fig. 1.

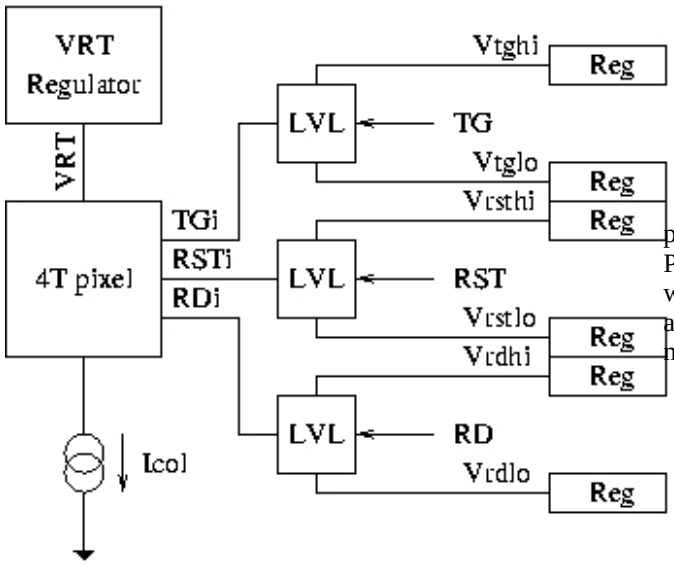

Figure 1. The pixel and its bias cells

Icol and VRT are used to bias the pixel's source follower. VRT is also used as the floating diffusion node reset voltage. Vtghi and Vtglo are used to bias the pixel's transmission gate. Vrsthi and Vrstlo are used to control the reset transistor, whereas Vrdhi and Vrdlo are used to control the pixel's read transistor. All these biases should be designed to operate at low current, and not introduce image artifacts.

How well a pixel rejects the non ideal behaviour of its biasing cells depends on its rejection to the various pixel supplies. There are two mechanism which limit the pixel rejection to its supplies: direct coupling for VRT, Icol, Vrdhi, and Vrdlo and clock feedthough for Vtglo, Vtghi, Vrsthi and Vrstlo. The rejection of the pixel is also influenced by the correlated double sampling (CDS) used in its timing, as shown in Fig. 2. As the readout will notice, all the references are CDS'ed except Vtghi and Vtglo.

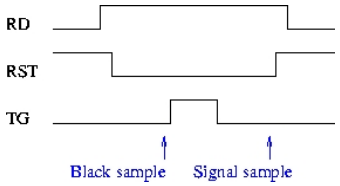

Figure 2. Timing of the pixel

II. PIXEL FPN

Pixel FPN describes the distribution of the DC offset from pixel to pixel, and is shown in Fig. 3 as a random distribution. Pixel FPN is linked to the quality of the CDS. For the CDS to work properly, one must ensure that the pixel settles properly alongside Vrdhi/Vrdlo, VRT and Icol during the two pixel measurements.

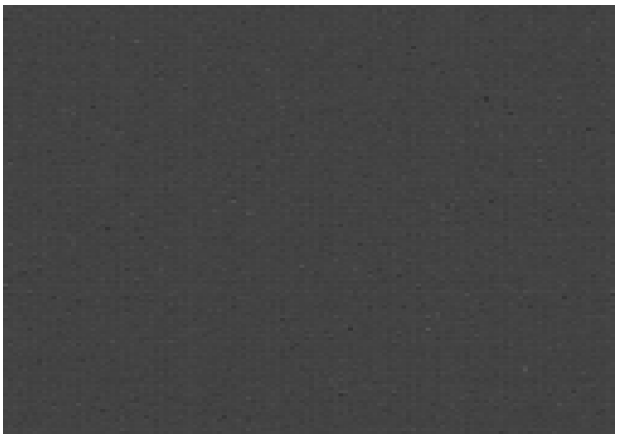

Figure 3. Pixel FPN

III. X AND Y DROOP

X or Y droop measure how the image behaves from left to right, or top to bottom. Ideally the image should be flat across all gains for a flat illumination scene. However, due to mainly track resistance and limitations in the impedance of the bias cells, a flat picture is difficult to obtain, especially for large arrays. The droop is often caused by two mechanisms: IR drops and RC time constants. It is easy to differentiate between both of them by slowing down the chip.

A. *IR based X-droop*

The main culprits for the IR based X droop is the routing for the VRT regulator and the routing for the column current source, as shown in Fig. 4. The drop in VRT from left to right causes an offset. The drop in Icol, causes a shift in the gain of the pixel source follower, which in turn leads to a droop.

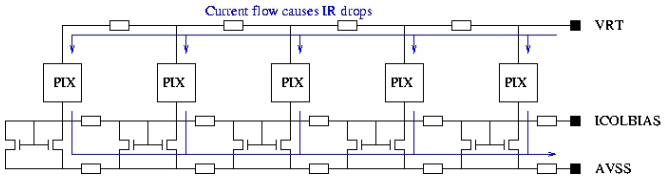

Figure 4. IR based X-droop

B. *Time constant based X-Y droop*

The time constant based X-Y droop is mainly caused by the delay of the TG, RD and RST tracks. However one must include into this delay the effects to the power tracks of vtghi,vtglo, vrsthi, vrstlo, vrdhi and vrdlo and the output impedance of the cells providing these biases, as shown in Fig. 5. The delay for the propagation of the pixel control signals must be low enough to ensure that the time constant induced offset does not introduce an offset in the image. The usual two main contributors are Vtglo and Vtghi, as CDS is not applied to them. The authors also note the poor rejection of the pixel to these biases.

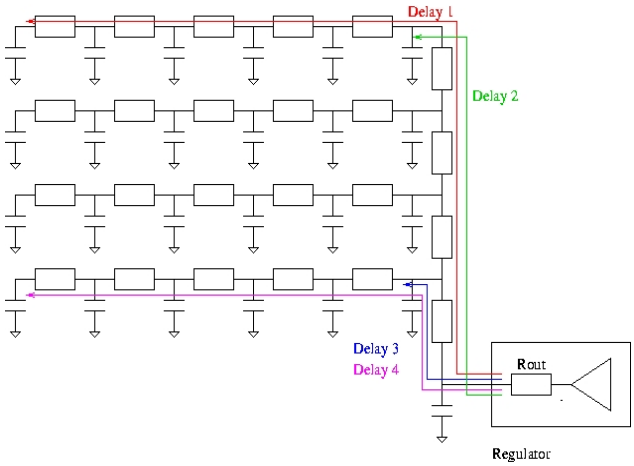

Figure 5. Time constant X-Y droop

IV. LINE BASED ARTIFACTS

A CMOS image sensor uses a rolling shutter type of readout. This makes it sensitive to pixel supply variation from line to line.

A. *Line FPN*

Line FPN has been observed in chips using a 1T75 pixel structure [2], as the source follower matching is often compromised to improve fill factor. These offsets often lead to a strong line fpn, as shown in Fig. 6. This fpn can be increased or decreased with icol, depending on its nature. An increase in Icol improves the pixel settling but also increases the vgs mismatch.

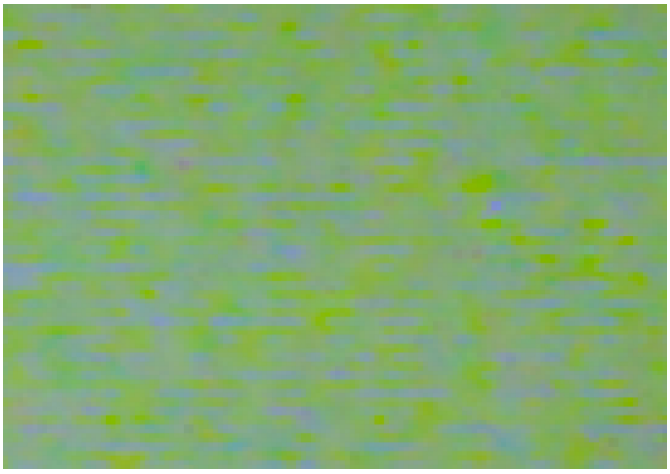

Figure 6. Line FPN after colour reconstruction

B. *Thermal line noise*

Thermal line noise is the random line noise, which is Gaussian in nature, as shown in Fig. 7. It can be caused by any of the biases, though often it seems Icol, Vtglo and Vtghi are the causes for this artifact. The reason for Icol is purely down to the fact that the pixel's source follower gm is sacrificed as the pixel gets smaller. This is not the case for the column current source thus any noise on the column current source bias is amplified on the pixel bitline. Vtglo and Vtghi are also contribute as the two signals are not CDSed.

Figure 7. Thermal Line noise

C. PSRR

Line noise caused by the power supplies has a beat associated to it. PSRR specs are especially stringent in mobile applications, as the supplies often jump up and down as appliances are turned on/off, and EM waves are picked up on the supply ring [3]. PSRR affects all references and the quality of the image is dictated by the weakest link. The line noise caused by PSRR is not random like thermal line noise, as shown in Fig. 8.

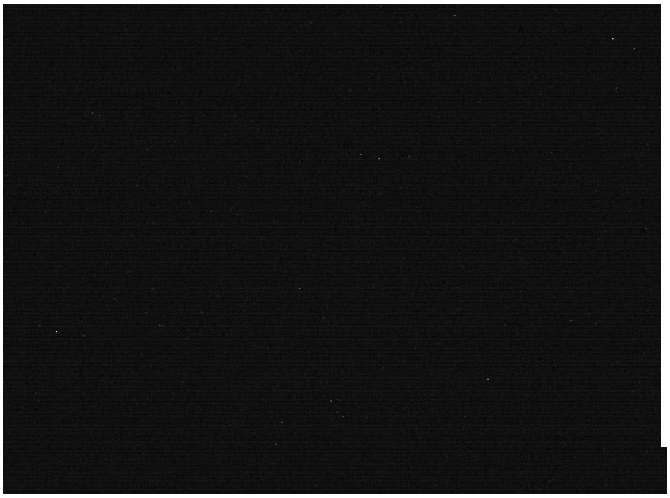

Figure 8. PSRR induced Line noise

D. FIBAR

FIBAR (Fixed Integration bar) is an image offset, which is dependant on the integration time used. The FIBAR issue, shown in Fig. 9 appeared with the usage of frame extension. In a low light environment, frame rate is reduced in order to increase integration time. There are two methods to do this: either reduce the system clock speed (clock derating), or increase the frame length (frame extension). Frame extension is the prefered option as it does not affect the quality of the CDS operation. The FIBAR, shown in Figure is caused by the fact that the kick on the supplies is not equal from line to line as shown in Fig. 10.

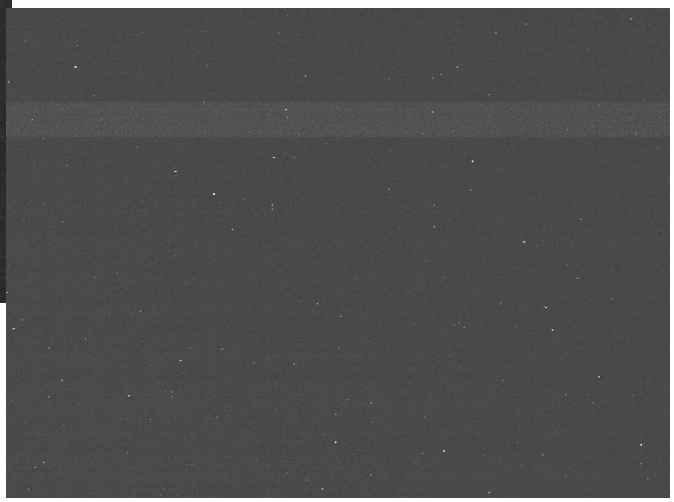

Figure 9. FIBAR in an image

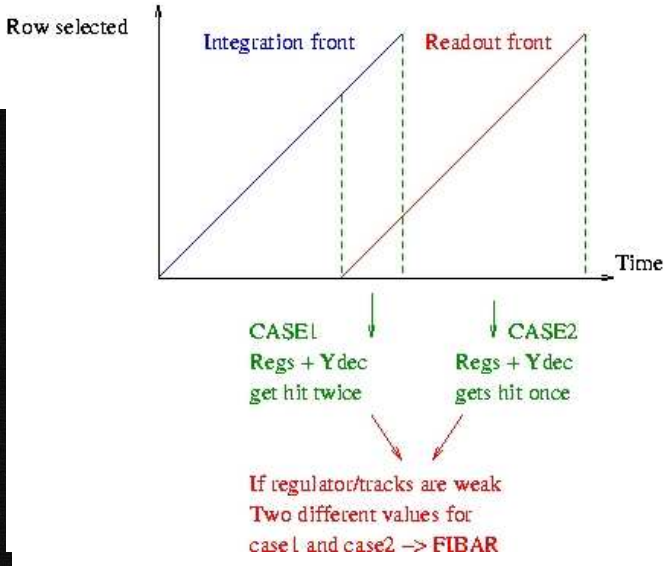

Figure 10. Explaining the FIBAR

The FIBAR phenomenon can be reduced by careful timing, but one must be careful not to increase the current consumption too much.

V. SMEARING

Smearing can be seen when a picture has a bright line on it, as shown in Fig. 11. In most cases it is caused by the quality of the ground plane of the sample and hold circuit. However

on more recent chips with high resolution it seems it is caused by the settling of the Vtglo regulator. The possible mechanism is shown in Fig. 12.

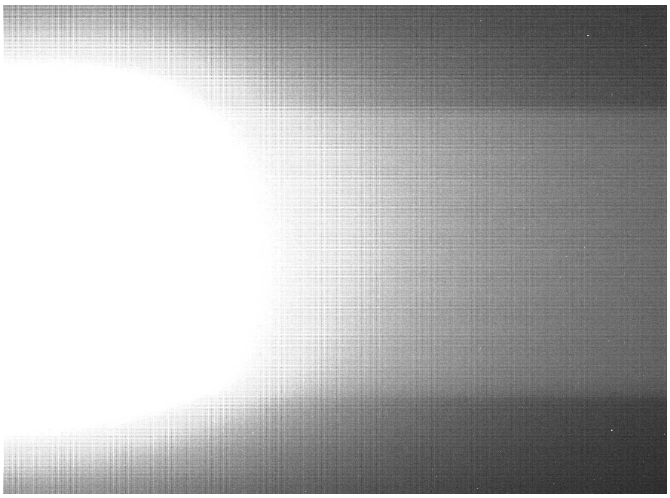

Figure 11. Smearing

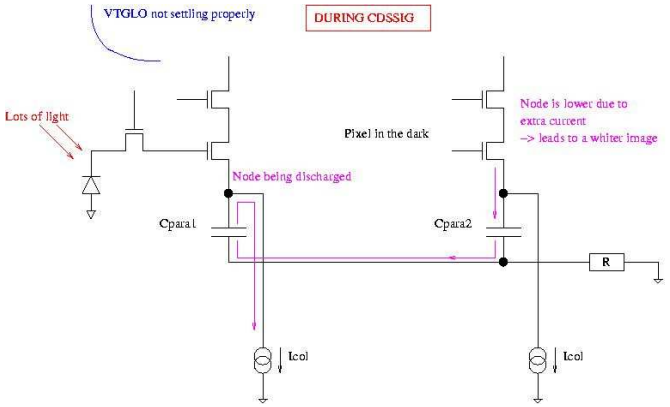

Figure 12. Vtglo contribution to smearing

VI. BLACK CHOPPING

Black chopping, shown in Fig. 13 occurs when the ground plane changes between the two cds samples, described in Fig. 14. The shift in the ground is caused by the power saving features on the regulators used to reduce overall current consumption. One must be careful about the settling of the ground plane with respect with the current kicks when powering on and off the pixel biases.

Figure 13. Black chopping

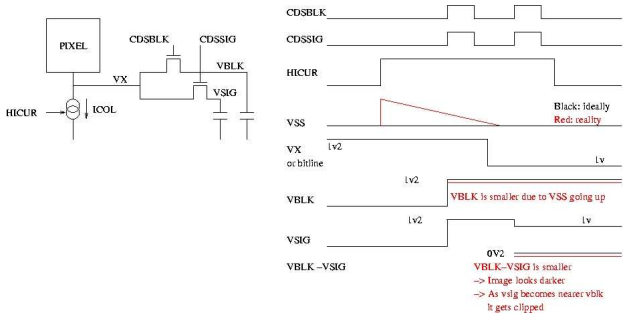

Figure 14. Explaining black chopping

VII. CONCLUSION

The main artifacts caused by the pixel bias cells have been presented. These artifacts can be reduced by correctly designing the bias cells so that their output impedance is low enough to avoid introducing x-y droop and smearing (Vtglo), their thermal noise low enough to avoid being above 1 code and their PSRR high enough to avoid seeing supply variations on the image. Layout is critical for x-y droop and reducing black chopping. The video timing was altered to remove FIBAR.

REFERENCES

[1] Shoji Kawahito, “Circuit and Device Technologies for CMOS functional Image Sensors”, VLSI 2006 IFIP International Conference, pp. 42–47, October 2006

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[3] Roberto Pelliconi and Nicolo Speciale, “Criteria to Reduce Failures Induced by EMI Conducted on the Power Supply Rails of CMOS Operational Amplifiers”, IEEE International Symposium on Electromagnetic Compability, pp.1102-1105 , Vol. 2, 13-17 Aug 2006