Progress in 1.25-inch Digital-Output CMOS Image Sensor Developments for UDTV Applications

I. Takayanagi, S. Osawa, T. Bales, K. Kawamura, N. Yoshimura, K. Kimura, H. Sugihara, E. Pages, A. Andersson, S. Matsuo, T. Oyama, M. Haque, H. Honda, T. Kawaguchi, M. Shoda, B. Almond*, P. Pahr**, S. Desumvila*, D. Wilcox*, Y. Mo***, J. Gleason***, T. Chow***, and J. Nakamura

Aptina Japan, LLC., * Aptina UK, Ltd., **Aptina Norway, AS., *** Aptina LLC, USA
Sumitomo Fudasan Mita Twin Building, East Wing 12F
Minato-ku, Tokyo 108-0023, Japan
+81-3-5439-3486, istakayanagi@aptina.com

I. INTRODUCTION

The Ultra-High Definition Television (UDTV) system is a next generation imaging system, featuring a wide viewing angle of 100 degrees with 4,000 scanning lines. Its image formats were standardized by ITU-R in July 2006 and are summarized in Table 1 [1]. Several prototype image sensors to realize the UDTV system were developed [2]-[6]. Among them, we have developed two 1.25-inch digital-output CMOS image sensors, referred to as UDTV1 sensor and UDTV2 sensor here. A 1.25" optical format with a 4.2μm pixel size has been chosen, because it does not require the stitching technique to fabricate the sensor chip while high quality images for a broadcasting use can be expected with a moderate pixel size of 4.2μm. A smaller camera system with much less power consumption has been built with the 1.25" format CMOS sensor, compared to a previous camera system with a 2.5" prototype CCD sensor [7]. The UDTV1 sensor, having 8.3M-pixels and operating at 60 fps, was reported in 2003 [3][4] and the improved version, UDTV2, was designed and built in 2007 [5]. In this paper, performance improvements in the UDTV2 sensor, compared to the UDTV1 sensor, are reported.

Table 1. UDTV image formats

Parameters	Systems	
	UHDTV1	UHDTV2 (SHV)
Pixel count	3840 (H)×2160 (V)	7680 (H)×4320 (V)
Image aspect ratio	16:9	
Frame rate and scanning	24, 25, 30, 50 60 fps progressive	
Sampling structure	4:4:4 for R, G, B 4:4:4 / 4:2:2 / 4:2:0 for Y, C_B, C_R	
Bit depth of pixel	10, 12	
Colorimetry	ITU-R BT.709	

II. UDTV1/ 2 SENSOR OVERVIEW

The image sensor architecture adopted for both UDTV1/2 sensors is shown in Fig. 1. The column parallel signal processing circuits, comprising a gain amplifier, a successive approximation analog-to-digital converter (SA-ADC) and digital memory banks, are arranged on the top and bottom sides of the pixel array.

The pixel and process technology are a 3-transistor photodiode pixel in a 0.25 μm 2P3M process for the UDTV1 sensor, and a 4-transistor pinned photodiode pixel in a 0.18 μm 2P3M CMOS process for the UDTV2 sensor, respectively. Specifications of the UDTV1/2 sensors are shown in Table 2.

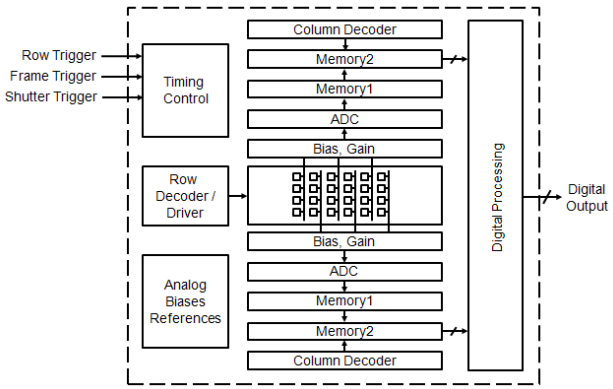
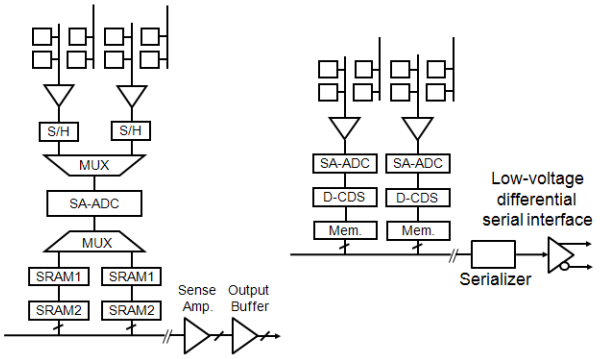


Fig. 1 Image sensor architecture

Table 2. Specifications of UDTV1/2 sensors

	UDTV1	UDTV2
Process	0.25μm 2P3M	0.18μm 2P3M
Optical format	1.25"	
Pixel size	4.2 μm	
Pixel type	3T PD	4T pinned PD
Number of effective pixels	3840 (H)×2160 (V) (8.3M-pixels)	4112 (H)×2168 (V) (8.9M-pixels)
Number of effective ADCs	1920	4112
Frame rate	60 fps	
ADC resolution	10b	12b (14b)
Output interface	Parallel 10b ×16 ports	Low-voltage differential 12b ×16 lanes
Input clock frequency	49.5 MHz	
Supply voltage	3.3 V	3.3V analog 1.8V digital
Package	262 pin PGA	164 pin PGA

Block diagrams of the signal chain for the UDTV1/2 sensors are shown in Fig. 2. It was expected that the use of a pinned photodiode pixel for UDTV2 sensor would reduce the noise floor drastically, which in turn would make fixed pattern noise (FPN) more visible. Thus, a digital correlated double sampling (D-CDS) scheme [8]-[10] was introduced in the UDTV2 sensor to suppress residual column FPN. A column amplifier is employed in both sensors to match the pixel signal range at low light conditions to the ADC input range and to reduce post-gain noise components (in this case, generated by the ADC) in the total input referred noise. A low voltage differential signaling output scheme is employed in the UDTV2 sensor, while a CMOS level parallel output scheme was used in the UDTV1 sensor.



(a) UDTV1 sensor (b) UDTV2 sensor

Fig. 2 Block diagram of signal chain

III. SIGNAL CHAIN OF UDTV1 SENSOR

In the UDTV1 sensor, one ADC is shared by two columns and laid out at four times the column pitch. Therefore, the number of total ADCs is 1/2 the number of pixel columns and two A/D conversions are needed in each row time. The signal chain and a row timing diagram of the UDTV1 sensor are shown in Fig.3 and Fig. 4, respectively.

The ADC is a charge re-distribution successive approximation ADC [11][12], which features low power consumption and moderate conversion time. The conversion time is 1.5µs for 10b conversion with a 49.5MHz clock, which is good enough for this particular application with the column parallel architecture (1 row time ~ 7.6µs). The area for the SA-ADC is determined primarily by the area for the bit capacitors. A use of binary scaled reference voltages is a technique to reduce the area for the capacitor banks [12]. Two reference voltages, i.e., V_{REF} and $V_{REF}/4$ are used for the SA-ADC in the UDTV1 sensor.

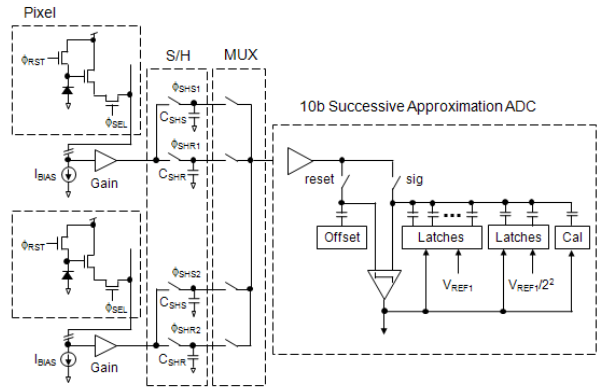


Fig. 3 Signal chain of UDTV1 sensor

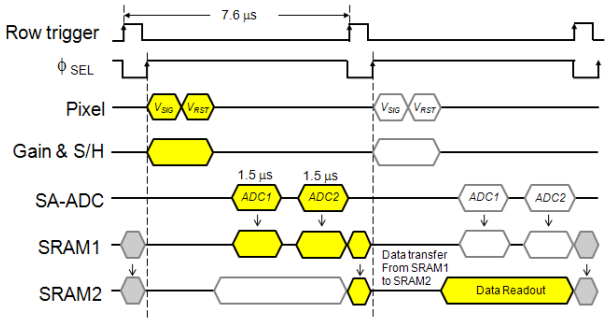


Fig. 4 Row timing diagram of UTDV1 sensor

IV. SIGNAL CHAIN OF UDTV2 SENSOR

The signal chain and a row timing diagram of the UDTV2 sensor are shown in Fig.5 and Fig. 6, respectively.

a. Pixel

The UDTV2 sensor employs a 4-transistor pinned photodiode pixel.

b. A/D Converter

The ADC resolution in the UDTV2 sensor is increased to 14b (from 10b in the UDTV1 sensor), though output resolution is limited to 12b in 60fps mode. With a finer process technology, one ADC can be laid out at two times the pixel pitch, thereby requiring only two A/D conversions in each row time for digital CDS. Three reference voltages, i.e., V_{REF}, $V_{REF}/4$ and $V_{REF}/16$, are used for the SA-ADC in the UDTV2 sensor.

Two A/D conversions are performed for digital CDS, as shown in Fig. 6. The first conversion is for the pixel reset level and is performed for the lower 12bits with its two most significant bits being set to "0". The second conversion is a 14b conversion for the pixel signal level.

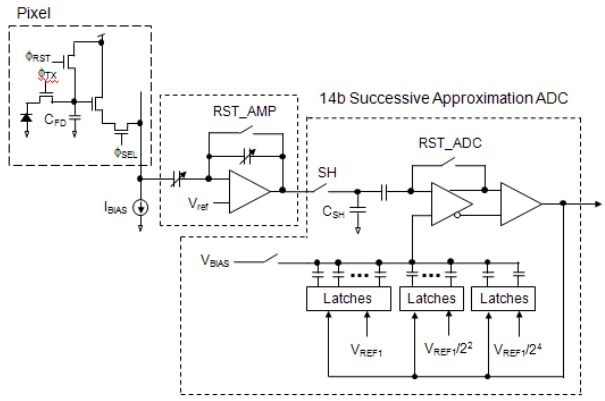


Fig. 5 Signal chain of UDTV2 sensors

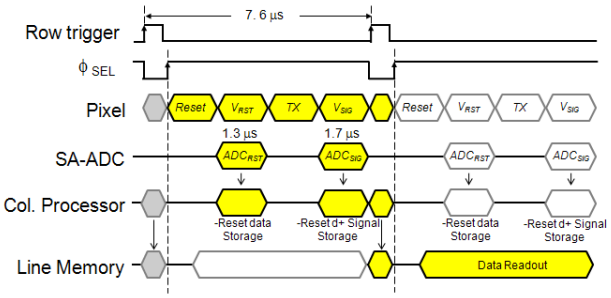


Fig. 6 Row timing diagram of UTDV2 sensor

c. Column Digital Processor and Line Memory

The column digital processor, labeled as "D-CDS" in Fig. 2 (b), performs digital CDS. The output of the SA-ADC is MSB-first 14bit serial data. As shown in Fig. 6, the column digital processor performs a "0 – Reset" operation during the first A/D conversion period in a row time and a "– Reset + Signal" operation during the second A/D conversion period. After the second operation is completed, the "– Reset + Signal" data is fed to the line memory. Data readout through the high-speed serial interface is performed during the next row period.

d. Output Interface

The low-voltage differential serial interface adopted in the UDTV2 sensor reduces both output pin counts and noise generation. A block diagram of the UDTV2 sensor including the digital data path and differential serial output blocks is shown in Fig. 7. 15b pixel data stored in the line memory is fed to the data path block where a digital pedestal is applied, a synchronization code is embedded during every horizontal blanking period, and the data is serialized. 16 data path and differential serial output blocks are implemented and each differential serial output block consists of 4 data lanes and 1 DDR (Double Data Rate) clock lane. The typical common mode voltage of the differential output is 0.2V and the differential output amplitude is 0.2V at a 100 Ω termination resistor. Since the maximum bit rate of the transmitter is 600 Mbps, only the upper 12bits of data are output (12b×49.5MHz = 594 Mbps) from the UDTV2 sensor to achieve 60 fps operation. (14bit full resolution data can be obtained in 50fps operation.)

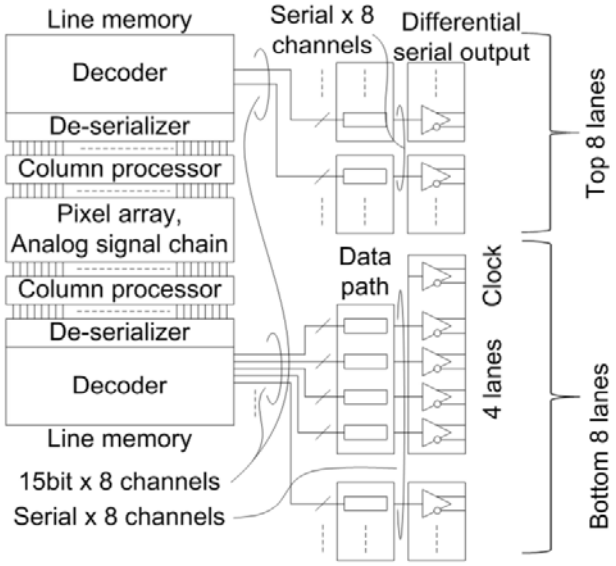


Fig. 7 Block diagram of UDTV2 sensor including digital data path and differential serial output blocks

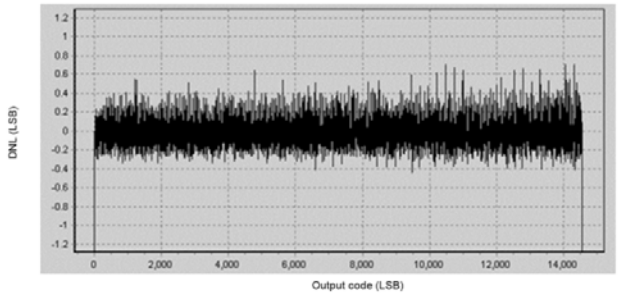
V. PERFORMANCE OF UDTV2 SENSOR

The differential non-linearity (DNL) and integral non-linearity (INL) of the 14b SA-ADC are shown in Fig. 8. The measurement was made with digital CDS operation. The DNL is within ±1 LSB for the entire output range. The power consumption of each ADC is 41µW.

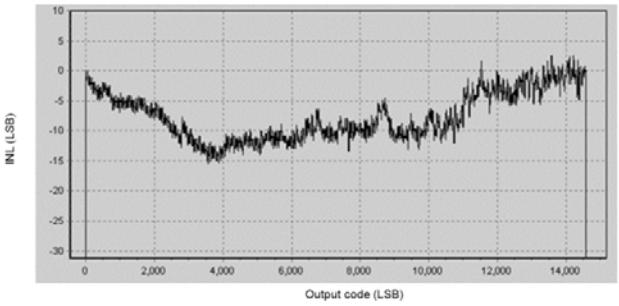
The performance comparison between the UDTV1 sensor [13][14] and the UDTV2 sensor [5] is shown in Table 3. A noise floor of 2.8 e^- at 8x column gain is obtained, which is approximately 15 times lower than that of the UDTV1 sensor, mainly due to a use of the pinned photodiode pixel. Digital CDS in the UDTV2 sensor successfully suppresses column-wise FPN caused by performance variation between the column parallel circuits. The column FPN of 0.36 e^-_{rms} is 1/7.8 the temporal noise floor of 2.8 e^-_{rms} and is hardly seen in the reproduced image. Also, row-wise temporal noise is suppressed by stabilizing a boosted voltage for the row select transistor inside the pixel by adding a decoupling capacitor.

The power consumption of the UDTV2 sensor is measured to be 1085 mW, which is about 500 mW higher than the UDTV1 sensor. This increase is primarily attributed to twice the number of the column amplifier and ADC and the addition of the on-chip Vref/Vbias generators,

while the power consumed by the output interface is decreased by using the low-voltage differential high-speed interface. Also, note that the power consumption of the output buffer in the UDTV1 sensor increases with the exposure level by up to 200mW because each data bit toggles more frequently. On the other hand, the power consumed by the low-voltage differential high-speed interface in the UDTV2 sensor is independent of the exposure level because of the current steering topology.



(a) DNL



(b) INL

Fig. 8 Non-linearity of the 14b SA-ADC

Table 2. Performance comparison

	UDTV1	UDTV2
Max handling charge (ADC limited)	25.0 ke$^-$	27.8 ke$^-$
Conversion gain	43 μV/e$^-$	45 μV/e$^-$
Noise floor	42 e$^-$	2.8 e$^-$ @8x gain
Row temporal noise	NA	0.57 LSB** 0.31 e$^-$ @8x gain
Total FPN	1.38 LSB* 23.6 e$^-$ @1x gain	0.65 LSB** 0.36 e$^-$ @8x gain
Column FPN	1.15 LSB* 19.6 e$^-$ @1x gain	0.65 LSB** 0.36 e$^-$ @8x gain
Pixel FPN	0.75 LSB* 12.8 e$^-$ @8x gain	-
Row FPN	0.12 LSB* 2.0 e$^-$ @1x gain	-
Power consumption	597 mW at dark	1085 mW

* in 10b ** in 12b

VI. CONCLUSION

Items that have been introduced to the UDTV2 sensor, compared to the UDTV1 sensor, include a 4-transistor pinned photodiode pixel, an increase in ADC resolution to 14b, a digital CDS scheme and a low-voltage differential signaling output scheme. The use of the 4-transistor pinned photodiode pixel resulted in a complete removal of kTC reset noise that was a dominant temporal noise source in the UDTV1 sensor (with the 3-transistor photodiode pixel), and a drastic reduction of dark current and hot pixels. Low-voltage differential signaling avoids noise emission from the CMOS level output buffers that was seen in the UDTV1 sensor. With these factors, a noise floor of 2.8 e^-_{rms}, row temporal noise of 0.31 e^-_{rms}, and column FPN of 0.36 e^-_{rms} at 8x column gain have been achieved, resulting in approximately 10 times higher camera sensitivity and enabling the removal of FPN suppression circuitry in the camera head.

References

1. ITU-R BT.1769 “Parameter values for an expanded hierarchy of LSDI image formats for production and international programme exchange”.
2. C. Smith, *et al.*, “An 8 M-CCD for an ultra high definition TV camera,” in *Program IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, pp. 175-178, 1999.
3. I. Takayanagi, *et al.*, “A 1.25-inch 8.3M pixel digital output CMOS APS for UDTV application” in ISSCC Dig. Tech. Papers, pp.216-217, 2003
4. S. Iversen, *et al*., “An 8.3-Megapixel, 10-bit, 60 fps CMOS APS,” in *Program IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, 2003.
5. S. Matsuo, *et al.*, “A very low column FPN and row temporal noise 8.9M-pixel 60fps CMOS image sensor with 14bit column parallel SA-ADC,” Symp. VLSI Circuits Dig. Tech. Papers, pp. 138-139, June 2008.
6. T. Yamashita, *et al.*, “Experimental color video capturing equipment with three 33-megapixel CMOS image sensors”, Proc. IS&T/SPIE Electronic Imaging, February 2009.
7. H. Shimamoto, *et al.*, "An 8K×4K Ultrahigh-Definition Color Video Camera with 8M-Pixel CMOS Imager", SMPTE Motion Imaging Journal, July/August 2005.
8. W. Yang, *et al.*, “An Integrated 800×600 CMOS Imaging System” in ISSCC Dig. Tech. Papers, pp.304-305, February 1999.
9. Y. Nitta, *et al.*, “High-speed digital double sampling with analog CDS on column parallel ADC architecture for low-noise active pixel sensor,” ISSCC Dig. Tech. Papers, pp. 500-502, February 2006.
10. S. Yoshihara, *et al.*, “A 1/1.8-inch 6.4Mpixel 60 frames/s CMOS image sensor with seamless mode change,” ISSCC Dig. Tech. Papers, pp. 492-493, February 2006.
11. Z. Zhou, *et al.*, “CMOS active pixel sensor with on-chip successive approximation analog-to-digital converter,” IEEE Trans. Electron Devices, vol. 44, pp. 1759-1763, Oct. 1997.
12. A. I. Krymski, *et al.*, “A high-speed, 240-frames/s, 4.1-Mpixel CMOS sensor,” IEEE Trans. Electron Devices, vol. 50, pp. 130-135, Jan. 2003.
13. M. Shirakawa, *et al.*, “Design consideration on FPN suppression circuit for 1 1.25” 8.3M-pixel digital output CMOS APS,” in *Program IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensors*, 2003.
14. I. Takayanagi, *et al.*, “A 1.25-inch 60-frames/s 8.3-M-pixel digital-output CMOS image sensor,” IEEE JSSC, vol. 40, no. 11, pp. 2305-2314, November 2005.