

# A Low Dark Count Single Photon Avalanche Diode Structure Compatible with Standard Nanometer Scale CMOS Technology

Justin A. Richardson, *Graduate Student Member, IEEE*, Lindsay A. Grant, *Member, IEEE*,  
and Robert K. Henderson, *Member, IEEE*.

**Abstract-** A single photon avalanche diode structure implemented in a 130nm imaging process is reported. The device employs a p-well anode, rather than the commonly adopted p+, and a novel guard ring compatible with recent scaling trends in standard nanometer scale CMOS technologies. The  $50\mu\text{m}^2$  active area device exhibits a dark count rate (DCR) of 25Hz at 20°C and a photon detection efficiency (PDE) peak of 28% at 500nm.

**Index Terms-** Biomedical imaging, CMOS integrated circuits, Image Sensors, Photodetectors, Photodiodes, p-n junctions.

## I. INTRODUCTION

Single photon avalanche diodes (SPADs) are well suited to low light level, time correlated applications such as fluorescence lifetime imaging microscopy (FLIM), fluorescence correlation spectroscopy (FCS), positron emission tomography (PET) as well as ranging and 3D cameras. Commercially available systems have tended to use sensitive charge coupled device (CCD) sensors or photo multiplier tubes (PMTs) that can be bulky, expensive and fragile. The appealing prospect of integrating arrays of single photon detectors, quenching, read-out and fast data processing electronics into a cost effective, dense, monolithic, solid state implementation demands low dark count SPADs with high quantum efficiency in advanced nanometer scale CMOS processes. The limitations imposed by the implant depths, doping concentrations and design rule restrictions in advanced CMOS processes have led to narrow depletion width devices being reported with high DCR [1,2,3] due to tunnelling, and low photon detection efficiency (PDE) [4,5]. Detectors with low DCR and high PDE have been reported in full custom [6,7] or high voltage processes [8,9,10]. However, such

processes are not optimal for large-scale, dense integration of fast on-chip data conversion or processing circuitry such as in-pixel active quenching, counters or time to digital converters (TDCs). To the authors knowledge this is the first SPAD structure to achieve sub-100Hz DCR compatible with general-purpose, foundry CMOS technologies without process modification.

## II. DEVICE STRUCTURE

We report a Geiger mode SPAD integrated in a 130nm imaging technology, although all implants used are available in a general-purpose version of the process. A passive quench component and readout buffer circuit are included on chip. Although the structure can be formed in any standard CMOS process, an associated loss in optical transmission efficiency can be expected if imaging specific layers are not used in the formation of the optical stack above the detector.

Due to the doping concentrations and implant depths for the sub 250nm processes which are required to implement dense digital circuitry, the depletion regions of implemented SPADs have narrowed and thus a major contributor to dark count has become tunnelling. As well as the side effects of high doping levels the use of shallow trench isolation (STI) in such processes is known to increase stress and charge traps thus increasing dark count and afterpulsing. The benefit of the use of STI is increased electrical and optical isolation between detector elements, so enhancing array spatial resolution [1].

A feature of CMOS process generations beyond 250nm is the presence of an optional deep N implant formed by a high-energy ion implantation step before n-well formation. This deep N implant is contacted by a ring of n-well and is normally used to completely enclose p-well regions in order to isolate NMOS transistors from the remainder of the substrate. The resulting triple well, twin tub process has been used in recent years to obviate increasing noise-coupling issues and improve latch-up immunity.

In this work, the SPAD cathode terminal connection is formed by N WELL with N+ contact, down to retrograde DEEP N WELL. The anode is created via the use of P WELL with P+ contact. The normal procedure of implanting either

Manuscript received April 8, 2009. J.A. Richardson and R.K. Henderson are with the Institute for Integrated Micro and Nano Systems, The School of Engineering, The University of Edinburgh, The King's Buildings, Mayfield Road, Edinburgh, EH9 3JL, UK.  
J.A. Richardson and L.A. Grant are with ST Microelectronics Imaging Division, 33 Pinkhill, Edinburgh, EH12 7BF, UK.  
(e-mail: justin.richardson@st.com).

PWELL or NWELL above DEEP NWELL is avoided in the guard ring area by use of an IMPLANT STOP layer. The result is a deep retrograde NWELL with low surface doping, increasing with depth. The doping profile has been confirmed via TCAD modelling. The cross section diagram is shown in Fig.1.

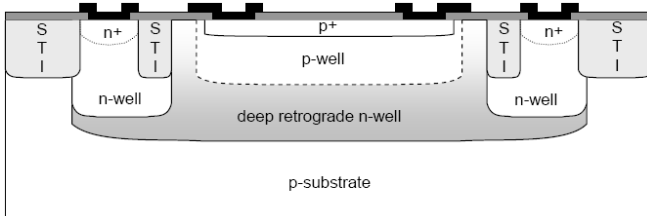


Figure 1: SPAD Cross Section

The result is a ‘virtual’ guard ring structure [6] but with a retrograde profile in the guard ring zone and without the use of an active region ‘enrichment’ implant. The PWELL anode forms a low field, deep junction (at depth  $\sim 0.5\mu\text{m}$ ) with a wide depletion region, greatly reducing tunnelling probability as well as broadening the wavelength response. An increased reverse breakdown voltage is observed compared to the conventional P+ anode structure [1-5], as expected.

It has been observed that in comparison with PWELL guard ring structures [2-5,8,10], ‘virtual’ guard ring structures such as reported in [6,7] and in this work are more amenable to spatial scaling due to the imposition of fewer design rule restrictions. This is advantageous when forming arrays of detectors. Additionally, [4] demonstrates that PWELL guard rings have a diameter limitation imposed by the merging of guard ring depletion regions. Compared to enrichment SPADs which require three implants (P+, NWELL and DEEP NWELL), the proposed SPAD forms both guard ring and breakdown junction simultaneously using only two drawn implants (PWELL and DEEP NWELL). The diameter of the PWELL offers a single parameter to scale the device active area.

### III. PHYSICAL IMPLEMENTATION

The schematic for the circuit implemented is shown in Fig 2.

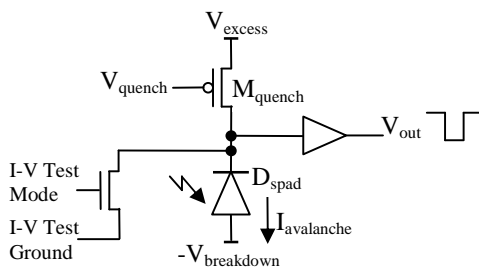


Figure 2: SPAD, Passive Quench and Output Buffer

The circuit used permits tuning of the detector dead time via control voltage  $V_{\text{quench}}$  from  $\sim 20$ -400ns. The control signal ‘I-V Test Mode’ allows for both I-V curve plotting and output buffering with one circuit at the expense of one minimum size source-drain diode capacitance on the circuit’s critical SPAD output node. The output buffer is a multi-stage inverter chain to enable fast driving of the parasitic capacitance on the IO pad associated with node  $V_{\text{out}}$ . The polygons that combine to create the  $8\mu\text{m}$  active diameter device are formed in an on-grid circular shape to minimise high corner fields and promote active region breakdown homogeneity. A photomicrograph of the device is shown in Fig. 3.

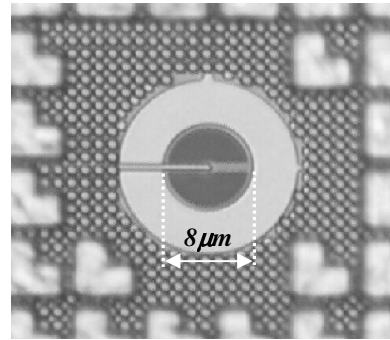


Figure 3: Fabricated Device Micrograph

The polygons shown surrounding the detector aid in meeting the layer density design rules required when using this process technology. These hide the integrated quench and readout buffer from view.

### IV. RESULTS

The device exhibited a sharp reverse I-V breakdown characteristic voltage of 14.4V with a dark current at the knee of less than 1nA, shown below in Fig. 4. Peaks in the response are due to semiconductor parameter analyser ranging disturbances.

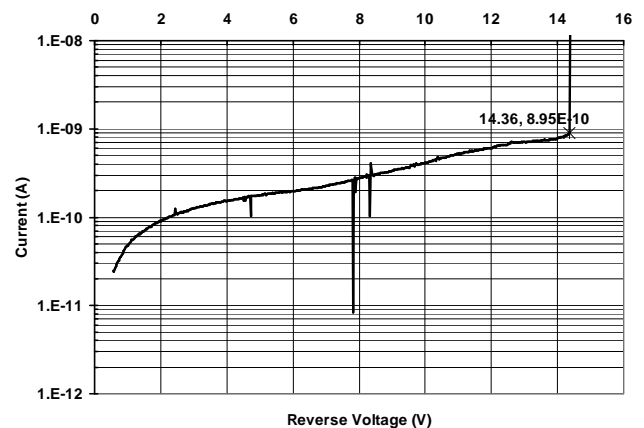


Figure 4: SPAD I-V Response

PDE is then plotted against incident wavelength for different excess bias voltages of 0.6, 1.0 and 1.4V (dotted line) with a detector dead time of 100ns. This is shown in Fig. 5. This shows a ripple characteristic in the response which is due to interference filter effects as the light is transmitted through the optical stack which consists of several layers with different refractive indices. The peak PDE of 28% is less than that reported in [2] but exhibits the intended broader response shifted toward the longer wavelength region but with a greatly reduced dark count.

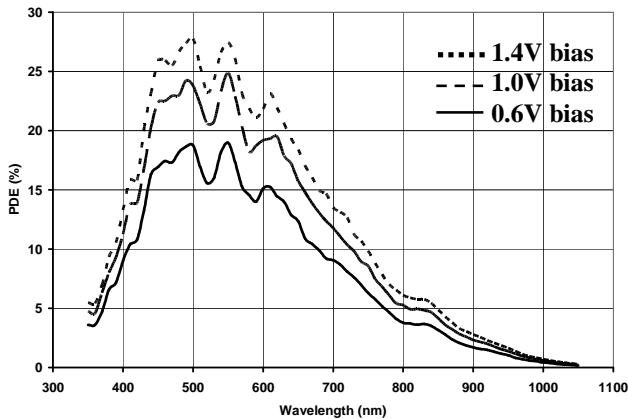


Figure 5: SPAD Photon Detection Efficiency versus Wavelength

The timing jitter is measured as ~200ps full width half maximum (FWHM) which is higher than that of [2,3] and is to be expected with a lower field P-N junction. This is shown in Fig. 6. at 100ns dead time for two different laser illumination wavelengths of 470nm and 815nm.

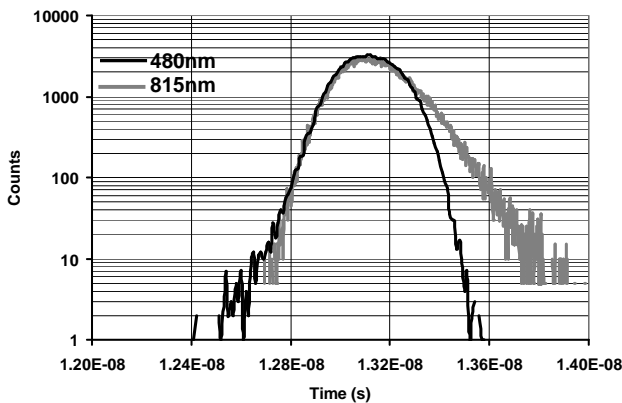


Figure 6: SPAD Timing Resolution

Although the FWHM figure remains the same, the extended diffusion tail exhibited during illumination by the longer wavelength pulsed laser source demonstrates that SPAD timing resolution is systematically wavelength dependent due to the absorption depth in silicon and should also be considered at for example 10% of FWHM.

The DCR of the device was measured over the temperature range -15°C to +45°C and is shown in Fig. 7 for three different excess bias levels. The slope of this graph suggests that at room temperature and above, the dominant source of dark count is thermal generation and not band-to-band tunnelling. The structure exhibits <20Hz dark count below 15°C ambient temperature.

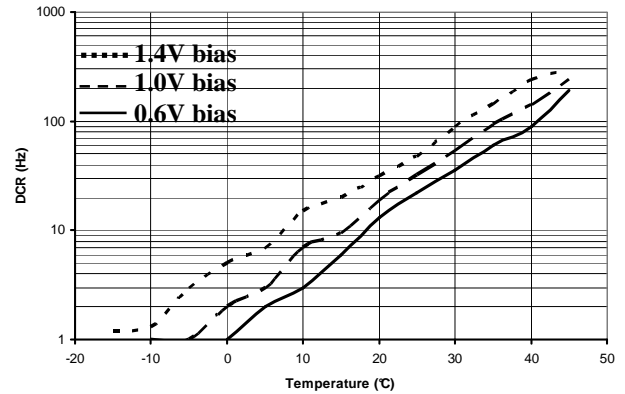


Figure 7: SPAD Dark Count Rate versus Temperature

DCR statistical spread over a 1024 element array biased at 0.6V excess bias is shown in Fig. 8. This shows approximately 80% of devices with DCR <150Hz, with a long tail of outliers up to several kilohertz, at room temperature.

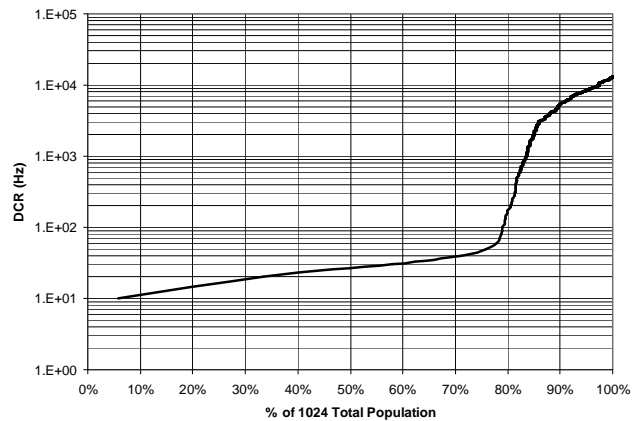


Figure 8: DCR Distribution

The device also exhibits a very low afterpulsing probability, achieved by minimising charge flow during breakdown to ~250ke at 1V excess bias, by keeping the moving node capacitance as low as possible [8] and the quality of the process technology which exhibits a low deep trap count. This is shown in Fig 9.

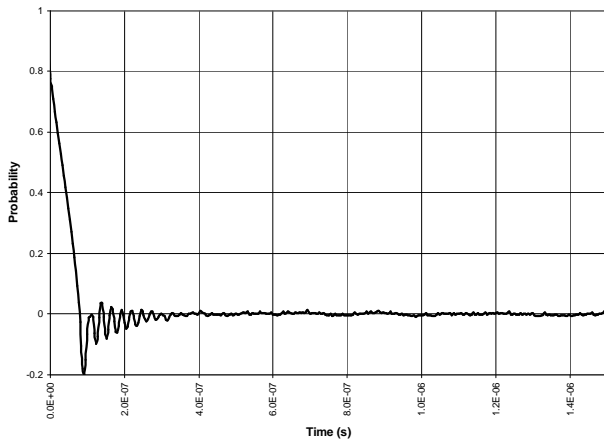


Figure 9: SPAD Afterpulsing Probability

Figure 9 is obtained by performing an oscilloscope autocorrelation measurement at room temperature. Slight ringing on the buffered SPAD output pulse disguises the critical time zone just after the first breakdown. However we observe at room temperature one afterpulse every 2-3 minutes of dark operation which corresponds to an approximate probability of  $\sim 0.02\%$ . Such a low probability indicates that space efficient and optimised passive quenching using a MOS element may be adequate in some TCSPC applications where the associated non-linear photon detection efficiency experienced during the SPAD's reset time can be accommodated.

## V. CONCLUSIONS

We have demonstrated a SPAD with low dark count and high PDE compared to other devices fabricated in comparable CMOS technologies [1-5]. The creation of a retrograde virtual guard ring SPAD with low DCR using standard process implants allows the implementation of large integrated arrays of detectors with fast quenching and readout circuitry. This work creates potential for the proliferation of low cost replacements for PMTs and CCDs, with system-on-chip (SoC) capability for scientific, medical and ranging applications.

## REFERENCES

- [1] FINKELSTEIN, H., HSU, M.J., ESENER, S.C.: 'STI-Bounded Single Photon Avalanche Diode in a Deep-Submicrometer CMOS Technology', *IEEE Electron Device Letters*, Vol. 27, Issue 11, 2006, p887-889.
- [2] NICLASS, C., GERSBACH, M., HENDERSON, R.K., GRANT, L., CHARBON, E.: 'A Single Photon Avalanche Diode Implemented in 130nm CMOS Technology', *Selected Topics in Quantum Electronics, IEEE Journal of*, Vol. 13, Issue 4, 2007, p863-869.
- [3] GERSBACH, M., NICLASS, C., CHARBON, E., RICHARDSON, J., HENDERSON, R.K., GRANT, L.: 'A Single Photon Detector Implemented in a 130nm CMOS Imaging Process', *Solid-State Device Research Conference, ESSDERC 2008, 38th European*, p270-273.
- [4] FARAMARZPOUR, N., DEEN, M.J., SHIRANI, S., FANG, Q.: 'Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18um Technology', *Electron Devices, IEEE Transactions on*, Vol. 55, Issue 3, 2008, p760-767.
- [5] MARWICK, M.A., ANDREOU, A.G.: 'Single photon avalanche photodetector with integrated quenching fabricated in TSMC 0.18um 1.8V CMOS process', *Elect. Letters*, Vol. 44, No. 10, 2008, p643-644.
- [6] LACAITA, A., GHIONI, M., COVA, S., 'Double epitaxy improves single-photon avalanche diode performance', *Electronics Letters*, Vol. 25, p841-843, 1989.
- [7] GHIONI, M., GULINATTI, A., RECH, I., ZAPPA, F., COVA, S., 'Progress in Silicon Single-Photon Avalanche Diodes,' *IEEE J. Sel. Topics in Quantum Electronics*, Vol. 13, p852-862, 2007.
- [8] ROCHAS, A., GANI, M., FURRER, B., BESSE, P.A., POPOVIC, R.S., RIBORDY G., & GISIN N., "Single photon detector fabricated in a complementary metal-oxide-semiconductor high-voltage technology," *Rev. Sci. Instrum.* Vol. 74, p3263-3270, 2003.
- [9] F. ZAPPA, S. TISA, A. GULINATTI, A. GALLIVANONI, AND S. COVA, "Complete single-photon counting and timing module in a microchip," *Opt. Letters*, 30, p1327-1329, 2005.
- [10] STAPELS, C.J., LAWRENCE, W.G., AUGUSTINE, F.L., CHRISTIAN, J.F., 'Characterization of a CMOS Geiger photodiode pixel,' *IEEE Trans. on Electron Devices*, ED-53, p631-635, 2006.