

# Ultra High Speed 3-D Image Sensor

Shingo Mandai<sup>†</sup>, Toru Nakura<sup>‡</sup>, Makoto Ikeda<sup>‡</sup> and Kunihiro Asada<sup>‡</sup>

<sup>†</sup>Dept. of Electrical Engineering and Information Systems, The University of Tokyo

<sup>‡</sup>VLSI Design and Education Center(VDEC), The University of Tokyo

2-11-16 Yayoi, Bunkyo-ku, Tokyo, 113-0032 Japan

Telephone: +81-3-5841-6771, Fax: +81-3-5841-8912

Email: mandai@silicon.t.u-tokyo.ac.jp

**Abstract**—We introduce the pixel parallel scan using light-section method by employing binary-tree priority encoder in each row and the pixel circuit which consist of current mode 1bit A/D converter, latch, and mask circuit to reset an activated pixel in each row and to search next activated pixel. We designed 256x256 image sensor using  $0.18\mu\text{m}$  CMOS process, and simulated the chip and evaluated the specifications of our sensor. In simulation, we realize 9.77K rangemaps/s. Furthermore, with high speed readout circuit, we will realize 78.1K rangemaps/s.

## I. INTRODUCTION

These days, 3-D movie and display technique have been developed rapidly, and have been applied as human interface or biometrics. However, higher and more accurate 3-D information acquiring techniques are required taking account of automatic robot control. There are many ultra high speed cameras with higher than 10,000 fps for specified usages. In fact, these camera can acquire only 2-D information, so if you want 3-D information, you should construct 3-D information from 2-D information employing the stereo-matching method. However, the stereo-matching method requires large resources and calculation time, so high speed real time 3-D construction is difficult. To solve this problem, many cameras using the time-of-flight(TOF) method have been developed[1][2], however, the TOF method has not realized high speed 3-D capturing yet because it is difficult to measure flight time in the usual background light and some TOF sensors need correlation. Then, some 3-D image sensor for the real-time 3-D construction employing the light-section method are presented[3][4]. The light-section method realizes high resolution and high speed 3-D construction because it is easy to detect a projected sheet beam and the range calculation is much easier than the stereo-matching method. However, the frame rate are restricted by the number of pixels in a column or a low linearly. Our presented 3-D image sensor employs pixel parallel scan using the binary-tree scan and the encoder in each row, and realizes the ultra high speed 3-D imaging. Our 3-D image sensor can also apply to multi slit light projection[5][6].

## II. SENSING SCHEME AND IMAGE SENSOR DESIGN

### A. Sensing Scheme Using Light-Section Method

Figure1 shows a system configuration based on the light-section method. The range finding system basically consists of a beam source, a scan mirror and an image sensor for position

detection. An image sensor detects the position of the reflected beam on the sensor array, and 3-D range data are calculated by the beam projecting angle and the beam incidence angle based on triangulation. The frame rate depends on pixel integration time and scan time to detect activated pixels on sensor array. Figure2 shows four search methods, a raster scan, a column parallel scan[3], a row parallel scan[4] and a pixel parallel scan. Raster scan is very slow, so a column parallel scan and a row parallel scan are often used for high speed range findings. However a column parallel scan and a row parallel scan are in proportion to the number of pixels in a column or a row. Actually, [4] employs asynchronous operation and realize high speed row parallel scan, but row parallel scan time depends on the number of pixels in a row linearly, and synchronous address encoding needs more time than the detection of an activated pixel. Our presented pixel parallel scan realizes a higher scan and address encoding at the same time.

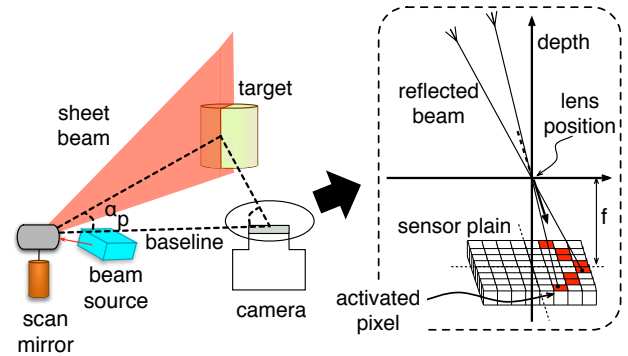


Fig. 1. System Configuration based on the light-section

### B. Pixel Parallel Binary-Tree Scan

Figure3 shows a block diagram of our chip. Pixel array has 256 x 256 pixels. Each row of pixel array has a binary-tree priority encoder[7]. After pixel array, 8 bit x 256 activated pixel addresses are readout to address encoder. The address encoder calculates a center of activated addresses when the number of readout pixel address is more than two, so encoded addresses are 9 bit x 256. Encoded addresses go to 48 parallel shift register for high speed readout to outside chip. Figure4 shows the binary-tree priority encoder embedded in a

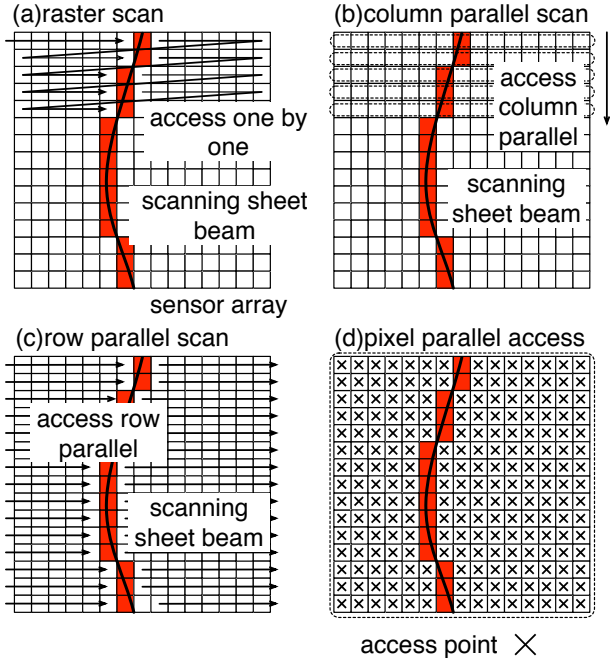


Fig. 2. Conventional scans for light-section method and a proposed scan

row. Binary-tree priority encoder searches most left activated pixel at first, and then, mask circuit in a pixel circuit resets the first detected pixel while detected addresses are set to the address encoder. After then, binary-tree priority encoder searches second activated address. This pixel parallel scan realizes the detection of an activated pixel in each row and the setting activated pixel address to the address encoder at the same time. When all activated pixels are detected, a finish frag is made, so we can move on to next sheet beam scan. Furthermore, because of the tree structure, this circuit can be designed in each row in a small way, in this case, we can design  $12\mu\text{m} \times 12\mu\text{m}$  with 20.0% fill factor for one pixel.

### C. Pixel Circuit

Figure 5 shows a pixel circuit. A pixel circuit consists of a photo-diode, a reference current source, a voltage amplifier, a latch, a mask circuit and a part of the binary-tree priority encoder. The photo-diode, the reference current source and the voltage amplifier operate as a 1bit A/D converter. At first, sw1 resets the photo-diode and inverter amplifier to cancel offset of an inverter amplifier, and an address reset signal reset pixel address lines. Secondly, the photo-diode starts integration and a voltage of node X rises or falls depending on the intensity of a projected sheet beam. Even if small voltage change of node X, voltage change of this node is amplified, so whether the beam is projected or not can be found. when sw2 is open, an amplified voltage is latched, and this operation is equally 1 bit A/D conversion. this latch threshold voltage can be changed by the voltage bias(vb). The role of the mask circuit is to reset the latch not to be detected again at next scan. This mask circuit make it possible to readout all pixel values in a row (usually

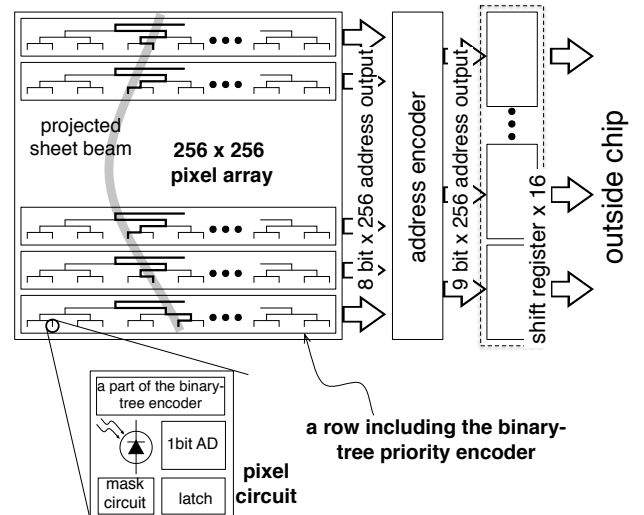


Fig. 3. Block diagram of a proposed sensor

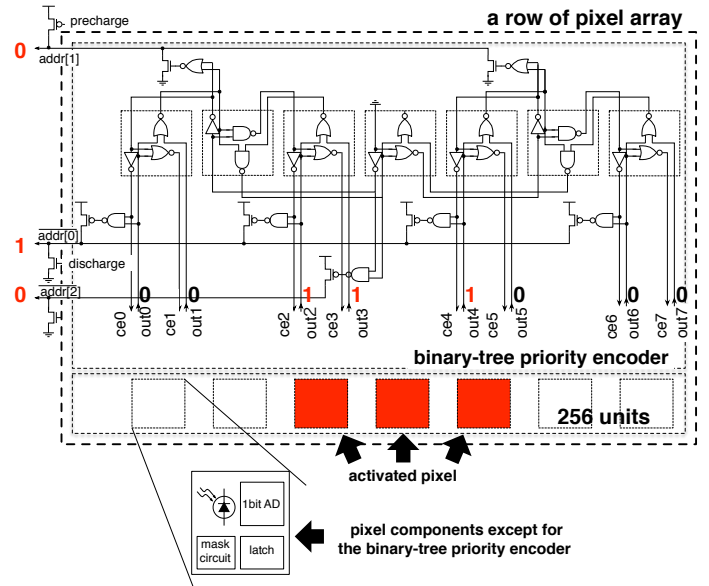


Fig. 4. Schematic of a binary-tree priority encoder embedded in a row of pixel array

at most about 5 activated pixels in one row). As a results, we can calculate the center of the projected sheet beam by using the address encoder. Figure 6 summarize a timing diagram.

### III. CHIP IMPLEMENTATION

A  $256 \times 256$  3-D image sensor using the present pixel-parallel scan has been designed and fabricated in a  $0.18\mu\text{m}$  standard CMOS process with 1-poly-Si 5-metal layers. This die size is  $4.9\text{mm} \times 4.9\text{mm}$ . Figure 7 shows the layout of our chip. The sensor consists of  $256 \times 256$  pixels, a reference current source, an address encoder and shift registers. The supply voltage is 1.8V. The size of a pixel circuit is  $12\mu\text{m} \times 12\mu\text{m}$  with 20.0% fill factor. It consists of a Psub-Nwell photo-

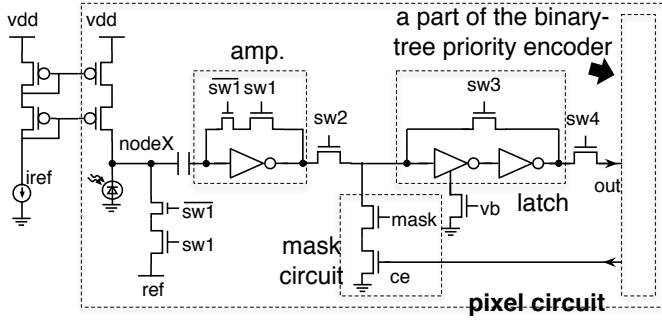


Fig. 5. Schematic of a pixel circuit

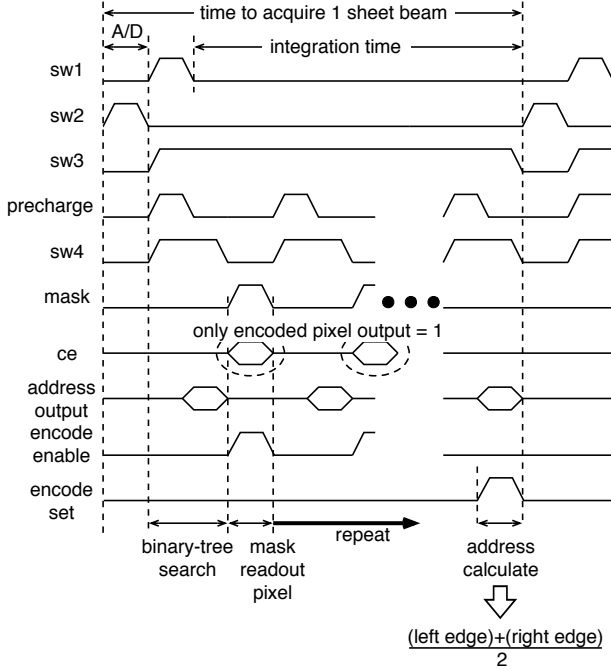


Fig. 6. Sensor operations and timing diagram

diode and 33 transistors and 2 gate capacitances. TABLE I summarizes the specifications of the fabricated chip.

#### IV. SIMULATION RESULTS

##### A. Performance Evaluation

Figure 8 shows voltage changes of the node X as the photo current changes and amplified voltage of the node X. The gain of this amplifier is 24.9 dB. When the sheet beam is projected, the photo current change from less than some hundreds pico ampere to some nano ampere. So, we simulate at the condition which the reference current is 1 nano ampere. As the simulation results shows, integration time is dependent on the photo current. If photo current is about 5nA, integration time is less than 100ns. Next, suppose that frame rate is restricted by the number of detected pixels and the time to read addresses outside chip. The 1bit A/D conversion takes 16.7ns, the binary-tree search needs 33.3ns, the mask operation takes

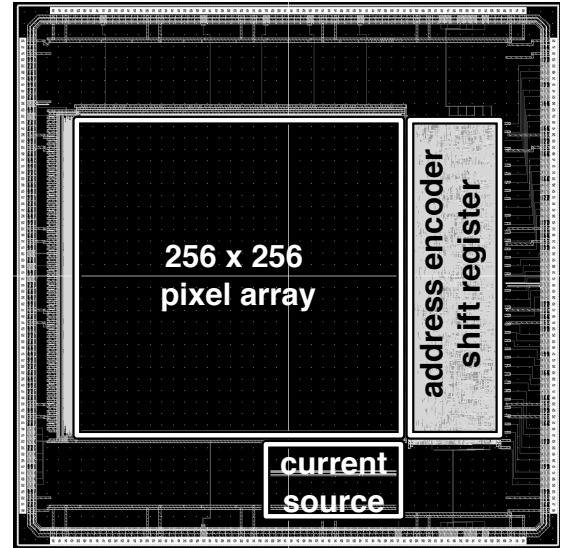


Fig. 7. Chip layout

TABLE I  
SENSOR SPECIFICATION(SIMULATIONS)

|                     |  |
|---------------------|--|
| Technology          | 1P5M 0.18 $\mu$ m CMOS standard process  |
| Chip size           | 4.9 $\times$ 4.9 $\mu$ m <sup>2</sup>  |
| # of pixels         | 256 $\times$ 256 pixels  |
| Pixel size          | 12 $\times$ 12 $\mu$ m <sup>2</sup>  |
| Fill factor         | 20.0%  |
| Pixel Configuration | 1 Psub-Nwell PD, 33 FETs & 2 gate cap./pixel   |
| Sensitivity         | 588mV/(lx $\cdot$ s) at 550nm  |
| System clock        | 60MHz  |
| Supply voltage      | 1.8V   |
| Range finding speed | 9.77K range maps/s<br>@ 400ns integration time at 256 scan lines<br>78.1K range maps/s (cannot readout)<br>@ 33.3ns integration time at 256 scan lines |

16.7ns, When 8 pixels are detected, one sheet beam detection takes 400ns. It corresponds to 9.77 rangemaps/s with 256 scan lines. When 1 pixels are detected, one sheet beam detection takes 50ns. It corresponds to 78.1 rangemaps/s with 256 scan lines, however this chip have not high speed readout interface, so we will not readout continuously.

##### B. Current Source Variations

The Reference current source value of a pixel circuit should be larger than photo current of a pixel circuit not projected by a sheet beam(background level) and should be smaller than that of a pixel projected by a sheet beam(activate level). Because the photo current of a photo diode is very small, current source transistors operate in subthreshold region. In this region, drain current is given by

$$I_{ds} \propto \exp(\Delta V_t(n \times U_t)) \quad (1)$$

$$n = \left(1 + \frac{C_d}{C_{ox}}\right) \quad (2)$$

$U_t$  equal to 26mV,  $C_d$  means depletion layer capacitance and  $C_{ox}$  is gate oxide capacitance. Equation 12 means that

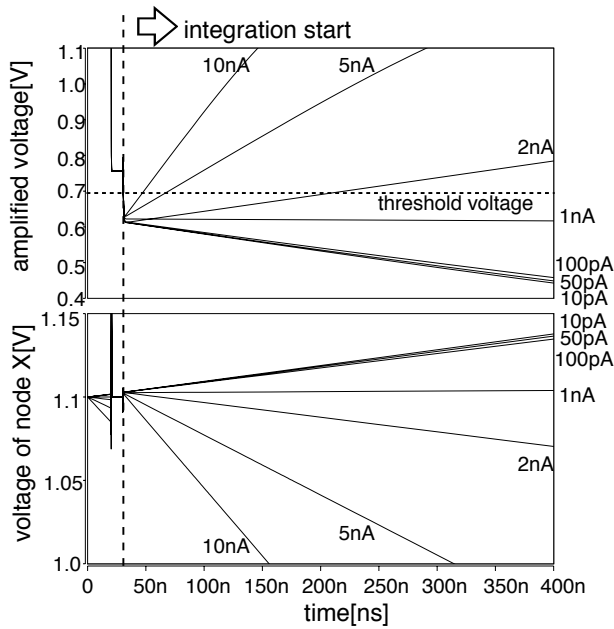


Fig. 8. Simulation results of node X and amplifier depending on beam intensity

threshold voltage variations effect a drain current in proportion exponentially. Figure9 shows the intensity profile of a projected sheet beam and the referent current source variations when threshold voltage changes by  $\pm 10mV$  using equation1,2. The margin to threshold should be kept for this chip to work correctly. Next step, To investigate the effect of variations of threshold voltage more precisely, we conducted montecarlo simulations by changing variation are of threshold voltage( $\sigma : 10mV$ ). As expected, much current variations are generated by the variation of threshold voltage of transistors of the reference current source. However, we can removed a wrong detection of not projected pixel by using mask circuit, and also overcome this error by using a stronger beam.

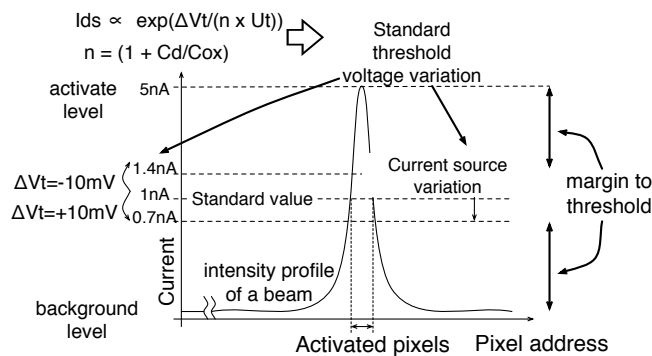


Fig. 9. Intensity profile of a projected sheet beam

## V. CONCLUSION

We introduce the pixel parallel scan method for light section method by employing binary-tree priority encoder every row

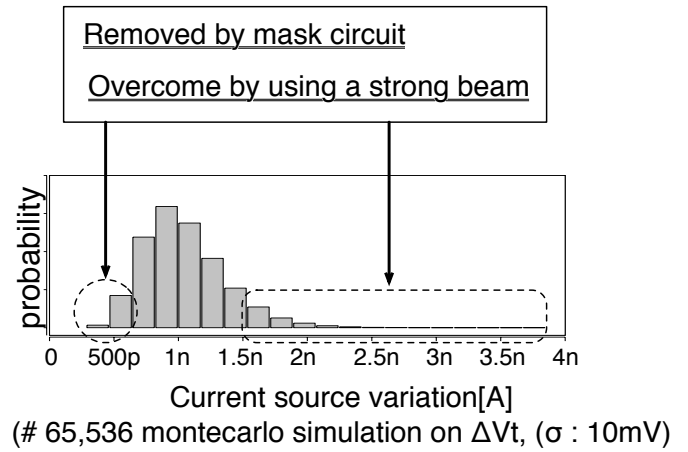


Fig. 10. FPN effect because of current source variations

and the pixel circuit which consist of current comparator, latch, and mask circuit to detect an activated pixel one by one at high speed. We designed 256x256 image sensor using 180nm CMOS process, and simulated the chip and evaluated the specifications of our sensor. In simulation, we realize realize 9.77K range maps/s. Furthermore, with high readout circuit, we will realize 78.1K range maps/s.

## ACKNOWLEDGEMENT

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