

High Speed Dual Port Pinned-photodiode for Time-Of-Flight Imaging

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ABSTRACT

Sensors for 3D vision open the way for new applications in video gaming, automotive, home TV, robotics. Today, Time-of-flight (TOF) is the easiest three-dimensional (3D) vision technique to implement and it offers good 3D reconstruction quality. TOF measurements based on a continuous-wave [1] or a pulsed [2] signal modulation are commonly used and often take advantage of a CMOS/CCD technology. However, the latter needs high voltages, induces high power consumption. Therefore there is a strong motivation for using advanced CMOS process and pinned-photodiode. Thus, pixel architecture developed in a 90nm CMOS image sensor technology and a high speed dual port pinned-photodiode optimized for light pulsed TOF (PLITOF) has been used.

I. PULSED LIGHT INDIRECT TIME-OF-FLIGHT PRINCIPLE

As explained on Figure 1, PLITOF principle consists in estimating the overlap between the received light pulse and the temporal window TG1. The ratio between the amount of collected carriers when TG1 and TG2 are respectively high is calculated to determine the distance [3]. The contributions of background light and dark current are removed by a correction using the same sampling scheme performed without illumination.

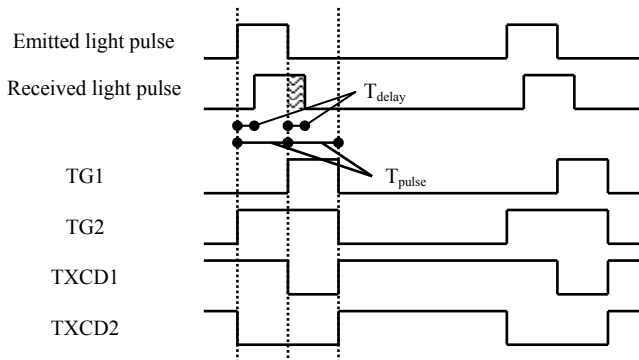


Figure 1: Pulsed Light Indirect Time-Of-Flight (PLITOF) principle

Calculated distance accuracy is determined after having made an optical power budget of the transmission chain and an uncertainty analysis. Shot noise, readout noise and quantization noise degrade the performance of the system.

Specific readout timing and an SRAM bank outside the chip must be implemented to remove kTC noise. The standard deviation of the distance after an average of 6 images has been plotted on Figure 2.

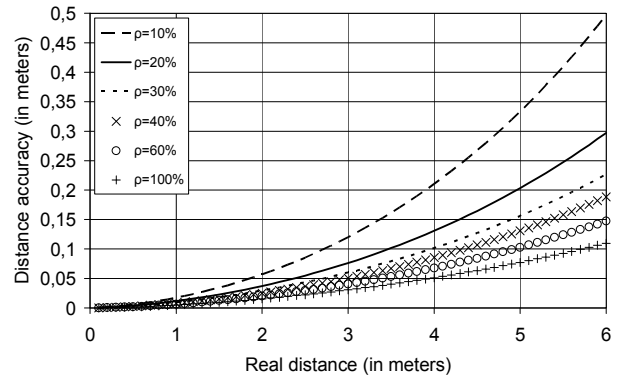


Figure 2: Theoretical distance accuracy as a parameter of the reflectance for 4W peak light pulses

Assuming the global noise follows a Gaussian law, the last results allow the investigation of a 3D reconstruction for a plane placed 3m away from the optical center and having a 40% reflectance. Distance accuracy has the best value at the center because it is especially the case where the distance travelled by the optical signal is the shortest (Figure 3).

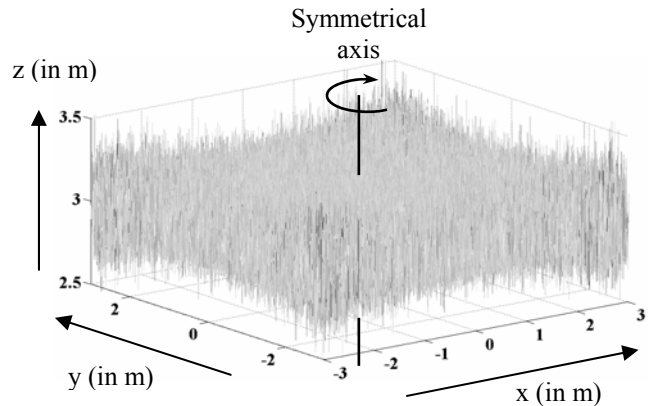


Figure 3: Simulation of a 3D reconstruction for a 3m away and 40% reflectance plane

II. PIXEL ARCHITECTURE

Due to the PLITOF principle, two pinned-photodiodes working in parallel are used. The first and second pinned-photodiodes respectively collect the electrons generated when TG1 and TG2 are high. For thermal dissipation considerations, small duty cycle must be applied. Thus when both TGs are low, a second transfer gate (TXCD) allows to drain all photogenerated electrons by background light to the power supply. Transit time of the electrons from the diode to the sense node must be compliant with the 50ns light pulse width. As shown on Figure 4, the 11.2 μm pixel is composed of two high speed dual port pinned-photodiodes.

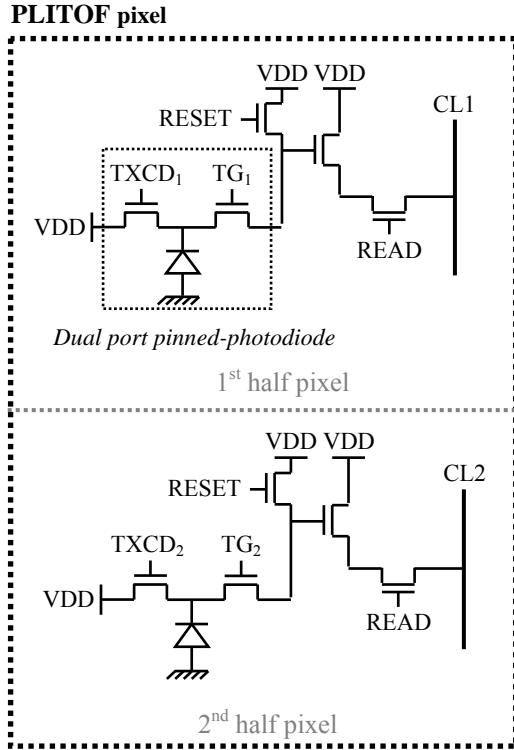


Figure 4: Schematic of the PLITOF pixel composed of two high speed dual port pinned-photodiodes

All photogenerated electrons must be driven from the generation site to the storage node in a few nanoseconds. Diffusion and electric drift are the two charge transport mechanisms. If both are considered separately, the transit time (TT) can be calculated in one dimension as a function of the pixel size and the silicon parameters [4].

$$TT_{\text{diffusion}} \approx \frac{\text{pitch}^2}{D_n} \quad (1)$$

$$TT_{\text{drift}} \approx \frac{\text{pitch}^2}{\mu_n \cdot \Delta V} \quad (2)$$

where D_n and μ_n are respectively the electron diffusion coefficient and electron mobility in silicon, pitch is the pixel size and ΔV is the potential difference between one side of the pixel (0V) and the position where the potential is maximum (pinning potential).

Moreover, when an 850nm light impacts the surface of the silicon, 83% of the flow is absorbed in the first 20 μm and only 41% is absorbed in the first 10 μm . Thus, a QE improvement at this wavelength and a short transit time about 10ns must be performed. As shown on Figure 5, QE in the near infrared (NIR) field has been increased by 11% thanks to a thicker epitaxial layer. A doping gradient in the epitaxial layer allows also the increase of the QE performance and the high speed transfer of generated electrons from the depth to the pinned photodiode depletion region.

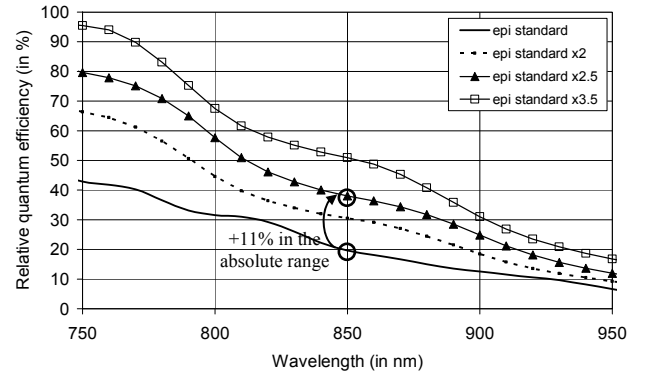


Figure 5: Measured quantum efficiency for several values of epitaxial layer thickness

The vertical drift created by the doping gradient is all the smaller because the epitaxial layer is thick. So, a trade-off between QE and transit time is necessary. An 8 μm thickness seems to be appropriate to our design (See Figure 5 and 6).

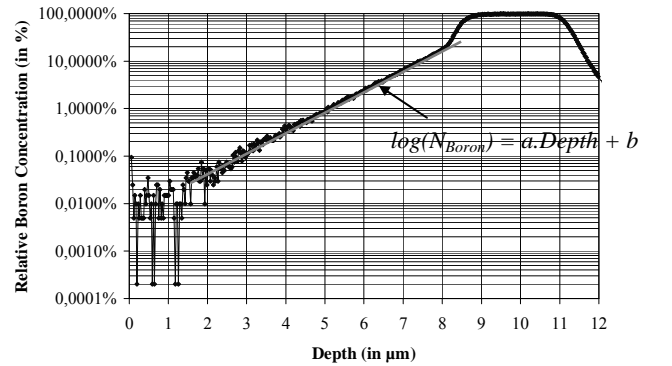


Figure 6: Relative Boron Concentration of the epitaxy

A cross-section and a potential diagram are shown on Figure 6.

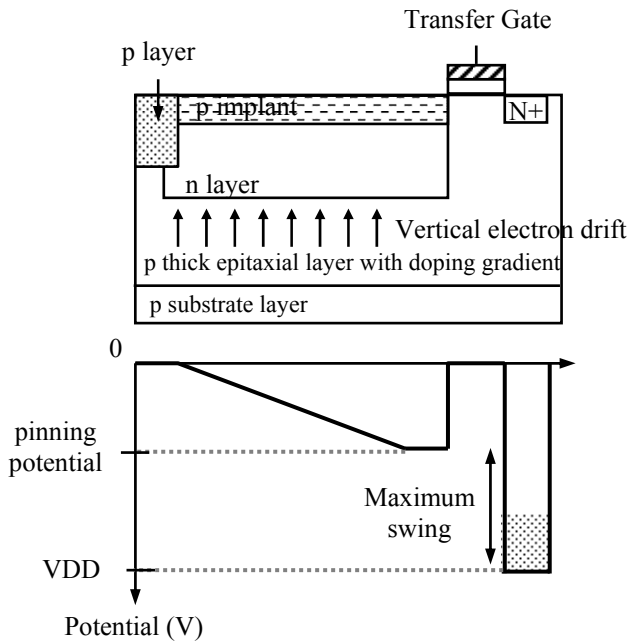


Figure 7: Cross-section of a half pixel

Likewise a pinning potential modulation generating a horizontal drift is created by a triangular shaped p-layer. It is better to generate a linear potential in order to drive electrons in the same way no matter where they are generated. Thus only one shape of the p-layer allows the generation of a linear potential inside the photodiode (See below Figure 8).

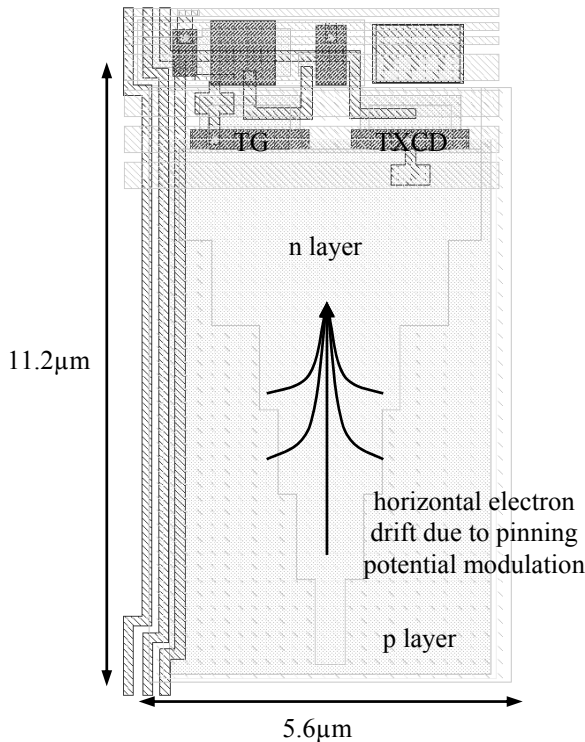


Figure 8: Layout of a half pixel

Array size is limited by the capacity to simultaneously drive the transfer gates of all the pixels due to the high oxide capacitance value, the resistance of metal layers and the need of global shutter mode. Indeed, when a rising or falling edge appears on the transfer gates, an extremely high current peak is observed on the power supply. Consequently, track width has been enlarged and bonding inductance has been reduced by the use of several leads in parallel. Decoupling capacitors have also been implemented. The layout of a 128 x 128 sensor designed in a 90nm CMOS image sensor technology is shown on Figure 9. The chip is currently being fabricated.

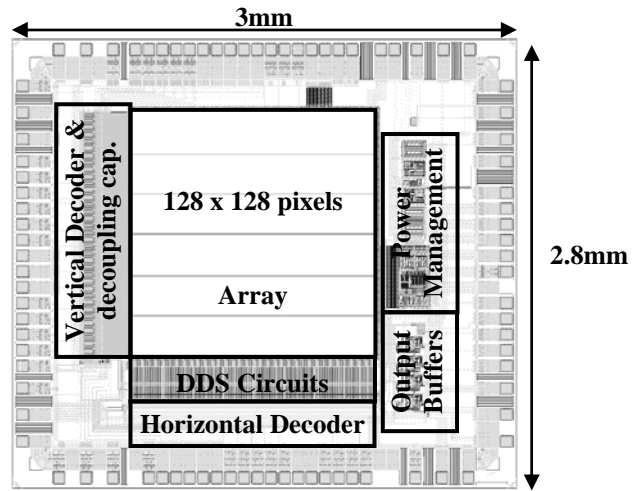


Figure 9: Layout of the 128 x 128 sensor

REFERENCES

- [1] T. Spirig, P. Seitz, O. Vietze, and F. Heitger, "The lock-in CCD two dimensional synchronous detection of light," *IEEE Journal of Quantum Electronics*, vol. 31, no. 9, pp. 1705–1708, September 1995.
- [2] R. Miyagawa and T. Kanade, "CCD-based range-finding sensor," *IEEE Transactions on Electron Devices*, vol. 44, no. 10, pp. 1648–1652, October 1997.
- [3] S. Kawahito, I. A. Halin, T. Ushinaga, T. Sawada, M. Homma, and Y. Maeda, "A CMOS time-of-flight range image sensor with gates-on-field-oxide structure," *IEEE Sensors Journal*, vol. 7, no. 12, pp. 1578–1586, December 2007.
- [4] B. Büttgen, T. Oggier, M. Lehmann, R. Kaufmann, and F. Lustenberger, "CCD/CMOS lock-in pixel for range imaging: challenges, limitations and state-of-the-art," Available: http://www.mesa-imaging.ch/pdf/RIM_Lock_In_Challenges_Limitations_5.pdf