High-saturation output 1.55-μm-square pixel IT-CCD with metal wiring line structure in a pixel

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Abstract

This paper describes the device performance of a 1.55-μm-square pixel interline transfer CCD (IT-CCD) having 12M pixels in a 1/2.3-inch optical format. The device has a novel metal wiring structure designed to increase the saturation signal that is determined by the effective supply voltage at the read-out gate, and employs a lateral overflow drain architecture to assist the low anti-blooming capability of the vertical overflow drain in the photodiode. As a result, we achieve a 14% higher saturation signal, and an anti-blooming performance that is 30-times superior to a 1.75-μm-square pixel CCD, despite the 27% smaller pixel area. These novel structures do not influence other performances of the device.

1. Introduction

Digital still cameras (DSCs) still need to produce high-quality images, even as their pixel size becomes smaller [1][2]. To maintain a high-quality image, it is important to keep a high signal-to-noise (S/N) ratio. The signal is determined by the saturation signal, which includes the capacitance of the photodiode (PD), the capability of the charge read-out from the PD to the vertical CCD (V-CCD), and the transfer capability at the V-CCD to the output circuit. In this study, we look at ways to improve the saturation signal at the PD, and the charge read-out capability from the PD.

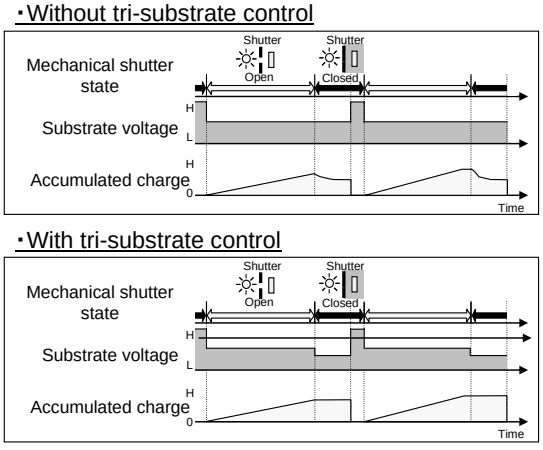


Fig.1 Exposure sequence at DSC

2. Charge accumulation capability in PD

At a small pixel size, the charge accumulation capability becomes smaller because it has a small static capacitance, which is limited by the PD area. Therefore, we improve the unit area charge accumulation ratio by using a shallow N-type diffusion area in the PD using a low-temperature process. Shallow N-type diffusion brings a higher unit area charge accumulation value, which is determined between this N-type region and the surface P-type area. This effect compensates for the decrease in area of the PD.

Another important task is to reduce the discharge phenomena caused by the vertical overflow drain (VOD) during the period the mechanical shutter is activated in DSC applications. (A DSC employs a mechanical shutter to control exposure time.)

During the mechanical shutter exposure period, the charge generated by incident light in the PD and the discharge quantity via the VOD are balanced. However, after the mechanical shutter closes, the accumulated charge in the PD decreases due to thermal hopping, despite the existing vertical overflow barrier (OFB). This means that the actual saturation signal, in other words the maximum accumulated charges in the PD, in a DSC is considerably lower than the theoretical static capacitance.

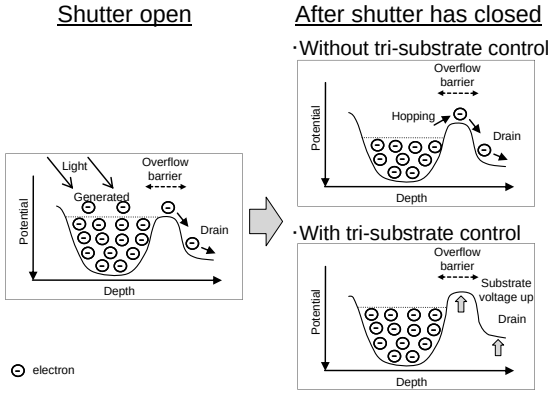


Fig.2 Potential profile of PD

Therefore, we adopt an additional device operation sequence called "tri-substrate control," which includes shutter operation, to obtain a higher saturation output for DSC applications. Figure 1 describes this operation method, and Figure 2 shows the effect of this sequence. The purpose of changing the substrate voltage after the mechanical shutter closes is to control the OFB potential height. Charge hop to the VOD via the OFB is prevented by the high potential barrier and accumulated charges are retained by this operation.

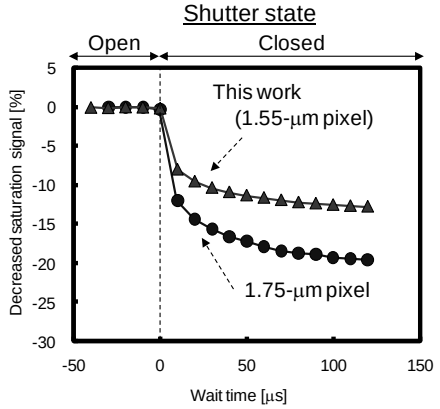


Fig.3 Time dependency of accumulation charge at PD

Figure 3 shows the result of the saturation-signal dependency on accumulation time, which includes the time for mechanical shutter operation. It indicates that the charge gradually decreases after the mechanical shutter has closed. It is observed that 87% of the charge still exists in the PD at the 100-μs point after the mechanical shutter has closed. The newly developed CCD has a lower discharge speed than that of the 1.75-μm pixel CCD. The cause of the lower discharge speed is the higher conductance resulting from the narrow channel effect in the overflow barrier between the charge accumulation region and the backside drain region.

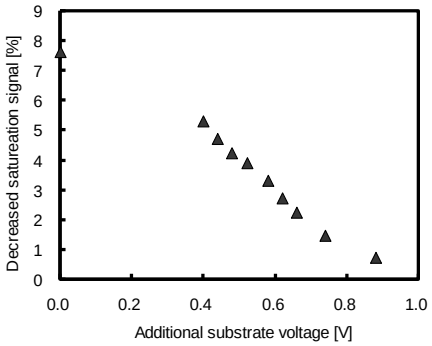


Fig.4 Additional substrate voltage dependency of accumulation charge at PD

Figure 4 shows the result of the saturation-signal dependency on additional substrate voltage. It has been observed that a higher substrate bias suppresses charge loss from the PD to the VOD, and it has been found that there is a linear relation between the amount of charge loss and substrate bias. This is a very useful relation with which to control actual saturation charge in a PD for DSC use.

3. Charge transfer from PD to vertical CCD

Supply voltage for charge transfer from the PD to the V-CCD is delivered by a poly-Si wiring line in previous devices. We chose a poly-Si wiring structure, because poly-Si material offers a lot of advantages compared to other materials, such as a lack of contaminants in the material, and the use of higher temperature fabrication process.

A narrower wiring line is required as a result of the miniaturization of compact DSCs, because a narrower wiring line can realize a low obstacle structure and achieve higher sensitivity. However, a narrower poly-Si wiring line decreases the charge transfer capability from the PD to the V-CCD, which mainly is determined by resistive-capacitive (RC) delay. The higher resistance of the wiring line increases voltage drop for the charge transfer operation. Hence, we could not supply sufficient bias, and thus could not read-out the charge from the PD to the V-CCD completely if a higher charge was stored in the PD.

To solve this problem, we used tungsten as a wiring material. Tungsten has low resistivity and a high melting point, and is used in semiconductor devices that need a high-temperature process (e.g. DRAM) [3]. Our CCD fabrication process requires high-temperature annealing due to the reduction of the interface state and the degree of noise from it.

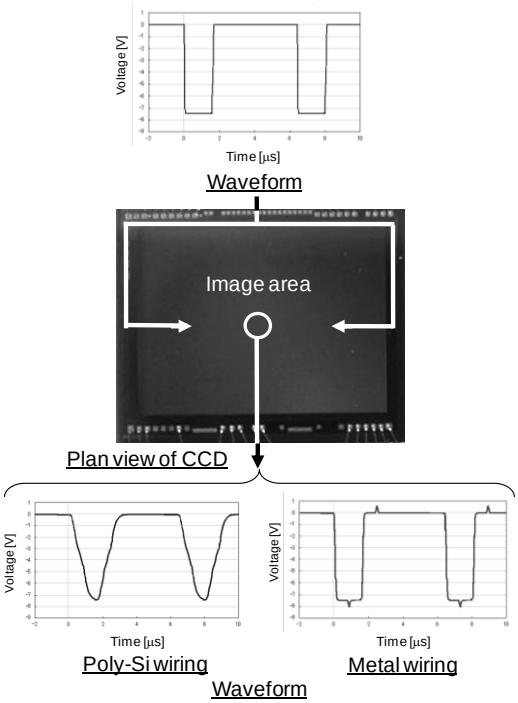
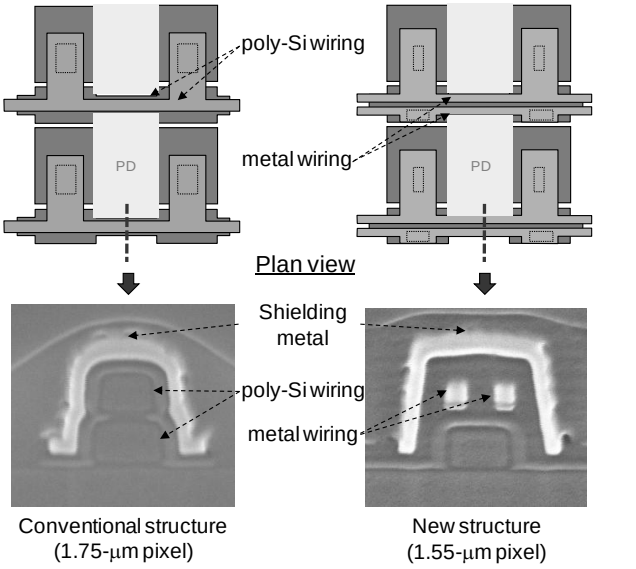


Fig.5 Simulation results of vertical CCD driving waveform (1/2.3-inch)

Figure 5 shows a simulation result of the supply

voltage waveform in a 12M pixel CCD that assumes the wiring materiel to be poly-Si and tungsten. The driving voltage is supplied from each side of the pixel array with a short Tr/Tf. With a poly-Si wiring line, the waveform at the center portion is collapsed from the rectangular, and the maximum supply voltage has reached only 0.1-μs. This is caused by the RC delay resulting from the higher wiring resistance. In contrast, with a tungsten wiring line, the waveform at the center portion is almost the same as the supply waveform at the outer pixel area, and the maximum voltage is reached almost at the same time as the supply voltage. This means that a lower resistance wiring line reduces RC delay and voltage drop.



SEM cross section (Voltage supply wiring line among pixels)

Fig.6 Comparison of wiring structure

Figure 6 shows the conventional and the newly developed wiring structures. The latter is composed of two parallel wiring lines made by the same tungsten layer. This structure was chosen from many candidate structures, as it is superior to the other structures in terms of optical performance and fabrication cost. These parallel tungsten lines lie on the poly-Si gate electrode and are covered with optical shielding metal. Each gate-electrode is connected via a wiring line through each contact. This mean that the metal wiring line is not a shunt wiring line, but a wiring line [4][5]. Therefore, this structure is not required to be buffered poly and should be able to handle a thicker gate poly-Si. The thickness of this metal wiring line is 90-nm and the layout pitch is 200-nm (Line/Space=90-nm/110-nm). These values are almost half those of a conventional poly-Si structure. However, the resistance of these metal wiring lines is 90% lower than in a conventional structure.

Figure 7 shows the complete charge transfer bias voltage dependency on the turn-on time of the read-out gate. This figure shows that conventional structure requires a 12.7V read-out voltage, but the newly

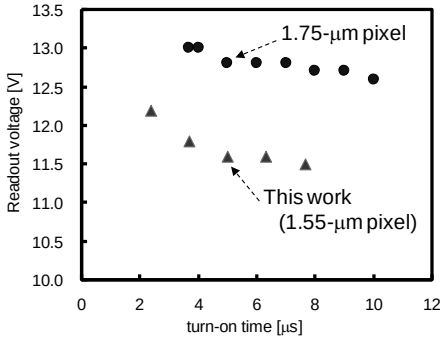


Fig.7 Readout voltage dependent on turn-on time

developed structure requires only 11.6V. This result demonstrates that a voltage drop of approximately 0.9V was achieved by the new metal wiring structure.

4. Saturation output signal

Figure 8 shows the trend chart of the saturation signal in SONY CCDs. The relative unit-area saturation signal of a 1.55-μm-square pixel CCD achieves a 43% larger saturation signal compared with a 1.75-um pixel. Actually, this represents a 14% larger saturation signal against a 1.75-um-square pixel CCD, despite the 27% smaller pixel size. The low-resistive wiring structure brings a higher-saturation output signal.

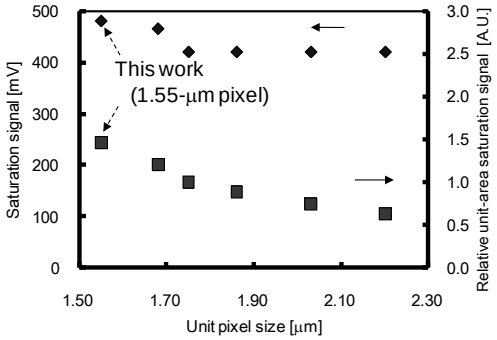


Fig.8 Trend of saturation signal

5. Lateral over flow drain

Conventional VOD architectures with small pixels (i.e. small PDs) have poor anti-blooming capabilities. The cause of this problem is the higher conductance resulting from the narrow channel effect in the overflow barrier between the charge accumulation region and the backside drain region. This narrow channel effect in the

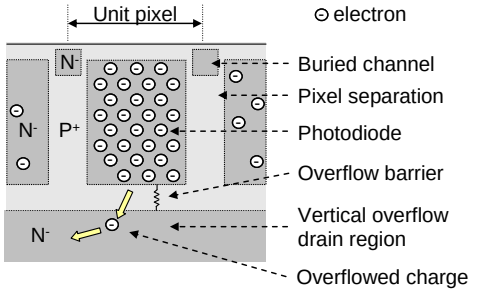


Fig.9 Cross section view of pixel in substrate

VOD is an unavoidable phenomenon in a small PD. (Figure 9)

Under high light conditions, the spilled charge from the PD will fill the V-CCD and neighboring pixels easier. The horizontal registers and Optical Black (OB) regions are also filled by the overflowing charge. If the charges overflow into the OB region, the signal level for the black level calculation becomes abnormal, and a pure black level is not reproduced.

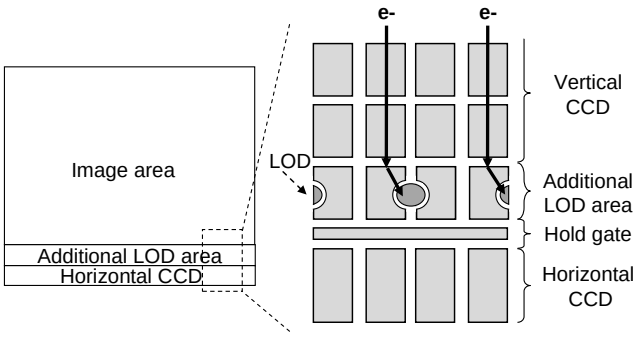


Fig.10 Schematic of lateral overflow drain

To avoid this phenomenon, we attach another blooming drain, a lateral overflow drain (LOD), that operates laterally and is located in the last V-CCD (Fig. 10). This lateral overflow drains the surplus charge away from the V-CCD when a certain level is reached, and prevents surplus charge overflow to neighboring pixels, horizontal registers, and the OB region.

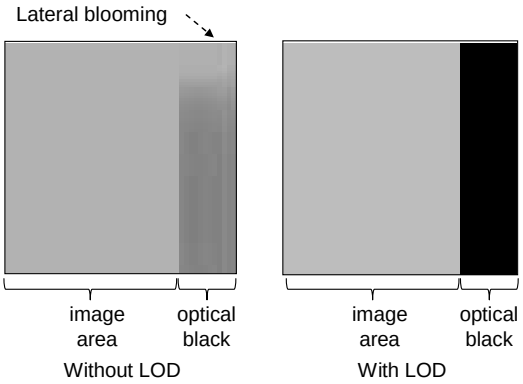


Fig.11 Comparison of anti-blooming capabilities

Figure 11 shows a captured image under high-light conditions. In the image to the left (without the LOD), the OB portion is white despite the fact there is no optical signal. This white OB region is generated by the spilled charge from pixels via the vertical register and neighboring pixels. In the image on the right (with LOD), there is no signal in the OB region. These figures show that the additional LOD in front of the horizontal resister works well and that the LOD compensates for the low anti-blooming capability. We achieve a 30-times higher anti-blooming capability compared with a 1.75-μm-square pixel CCD, which does not have a LOD architecture.

6. Conclusion

The novel metal wiring structure and anti-blooming architecture presented in this paper have been developed and verified on a 1.55-μm-square pixel IT-CCD image sensor with 12M pixels in the 1/2.3-inch optical format. We achieved a 14% higher saturation signal, and an anti-blooming performance that was 30-times superior to a 1.75-μm-square pixel CCD. The performance of this newly developed device is suitable for small-pixel image sensors, especially in DSC applications.

Table 1 Specifications and characteristics

Parameters	1.75-μm pixel	1.55-μm pixel
Wiring material	Poly-Si	Tungsten
Optical format diagonal [mm] ([inch])	7.183 (Type 1 / 2.5)	7.791 (Type 1 / 2.3)
Number of active pixels	3298 × 2472	4000 × 3000
Pixel size [μm×μm]	1.75 × 1.75	1.55 × 1.55
Vertical transfer speed [μs/line]	2.7	1.2
Holizontal clock rate [MHz]	36	38
Saturation output [mV]	420	480
Sensitivity [mV]	150	180
Support movig image mode	VGA / 30P	720 / 30P

7. Acknowledgement

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8. References

[1] Y. Kitano, et. al. "A 1.75-μm-square pixel IT-CCD having a gate oxide insulator composed of a single-layer electrode structure," IEEE 2007 INTERNATIONAL I MAGE SENSOR WORKSHOP, pp. 9-12, 2007

[2] N. Karasawa, et. al. "A 2.20-μm-square pixel IT-CCD constructed from a single-layer electrode," IEEE Workshop on CCD and Advanced, Image Sensor, pp. 210-213, 2005

[3] H. K. Kang et. al. "Highly Manufacturable Process Technology for Reliable 256 Mbit and 1 Gbit DRAMs," IEDM, pp. 635-641, 1994

[4] K. Yonemoto, et. al. "A 2 million pixel FIT-CCD image sensor for HDTV camera system," IEEE ISSCC, vol. XXXIII, pp. 214 – 215, 1990

[5] M. Mori, et. al. "A 2 M Pixel HDTV Image Sensor with Tungsten Photo-Shield and H-CCD Shun Wiring," ISSCC, vol. XXXIII, pp. 172-173, 1992