Design and Characterization of Submicron CCDs in CMOS

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Abstract

Three types of submicron CCDs are implemented in single-poly 0.11μm CMOS technology to demonstrate the feasibility of multi-aperture imaging systems that produce data from distributed arrays of CCDs integrated across a monolithic substrate. Test structures comprising 16×16 pixel Frame-Transfer (FT)-CCDs with $0.5 - 0.7\mu$m pixels are fabricated under various process conditions to implement devices which operate as surface-channel, buried-channel and pinned phase buried-channel. Ripple charge transfer and single electrode charge confinement are implemented to minimize pixel pitch.

Introduction

As pixel size is approaching the limits of conventional optics, improvements in resolution are diminishing. Scaling pixels beyond these limits, however, can provide new imaging capabilities beyond merely attempting to increase spatial resolution. In [1], we describe a multi-aperture approach to imaging, whereby the image sensor is partitioned into an array of apertures, each with its own local subarray of pixels and image-forming optics. A real image is focused a certain distance above the sensor such that the apertures capture overlapping views of the scene. The subimages are post-processed to obtain both a high resolution 2D image and a depth map. A key feature of this design is in the use of submicron pixels to obtain accurate depth measurements derived from the localization of features within adjacent subarrays. Other benefits of this configuration include the ability to image objects at close proximity to the sensor without the need for objective optics, achieve nearly complete color separation through a per-aperture color filter array, relax the requirements on the camera objective optics, and increase the tolerance to defective pixels. The architecture is also highly scalable, making it possible to increase pixel counts well beyond current levels.

Building submicron CMOS pixels with acceptable imaging performance at wide apertures is challenging because of the high dielectric stack height and optical occlusions resulting from the use of metal layers in the pixel. It has recently become possible to implement deeply scaled CCD pixels in modern CMOS due to the narrow poly gap spacing. This eliminates the need for processing multi-layer polysilicon and allows for electrode widths roughly equal to the gap spacing, which increases the effective quantum efficiency. Since the poly gap region normally creates either a pocket or a barrier, we make use of this feature to achieve single electrode charge confinement. The need for anti-blooming and high charge transfer efficiency are relaxed by the multi-aperture architecture where smaller subarrays are distributed globally.

This paper presents the design and characterization of 3 types of CCD structures implemented in 0.11μm CMOS technology: surface-channel, buried-channel, and pinned phase buried-channel. Each CCD structure differs in the location of charge storage during the integration time and in the sequencing of the electrodes during charge transfer. Our surface-channel design at 0.5μm pixel pitch was first reported in [2]. We used the buried-channel CCD design in a multi-aperture image sensor reported in [3]. A new pinned phase buried-channel design is implemented to improve both dark current and charge transfer efficiency. We use the poly gap region as an area for self-aligned implantation to create barriers that allow for inversion of the channel during the integration period. To characterize our designs, we fabricated test structures comprising arrays of 16×16, pixel FT-CCDs, each with source follower readout. We first discuss the design, fabrication, and operation of the image sensor, and then present simulation and characterization results.

Design, Fabrication, and Operation

We use an FT-CCD architecture to minimize pixel pitch and to eliminate metal layers in the active imaging area. We make the format of each sensor approximately equal to the dielectric stack height, which enables f/1 scale apertures for high sensitivity. We take advantage of the fact that the image capture is a distributed process by partitioning the subarrays into regions of high fill factor and occlusion free optical paths. Implementing the CCDs in CMOS enables fast multi-array readout along with the integration of analog and digital circuits. Each test structure consists of a pixel array, a storage array, a horizontal (H)-CCD, and a source follower readout circuit (see Fig. 1). The storage array is covered by metal layers that are also used to distribute global control lines (see Fig. 2). A photomicrograph is shown in Fig. 3. Each pixel consists of a single poly electrode, a channel, and a channel stop. The channels and stops for the surface-channel devices are shown in Fig. 4. The electrodes are patterned with non-silicided polysilicon as shown in Fig. 5. Each pixel array is separated by a wall of 4 metal layers. The first 2 metal layers are shown in Fig. 6.

In all designs, the polysilicon is doped by masking out the channels as shown in Fig. 7. The resolution of the S/D implant masks were the limiting factor in scaling beyond 0.5μm pixel pitch at this process node. We expect that it is possible to pre-dope the polysilicon before etch to scale the pixel size further. The polysilicon for the surface-channel device is doped N+ and the buried-channel designs are doped P+ to shift the workfunction closer to the operating range of CMOS circuits. The IOs on the test chip were designed to allow both positive and negative voltage sequencing. SEM images for each cross section of the surface-channel device are shown in Fig. 8 and Fig. 9. An electrode spacing of 180nm was used in all designs. The polysilicon is 130nm thick with gate oxide of 8nm. The channel stop for the surface-channel device is Shallow Trench Isolation (STI). The channel stop for the buried-channel is formed by a P-type implant (BF2, 75keV, 4.0E13/cm^2). The SEM for the H-CCD with fill-and-

spill input and floating diffusion is shown in Fig. 10. The required sequencing for this design is described in [3].

The pinned phase buried-channel design is shown in Fig. 11 with doping profiles plotted in Fig. 12-13. This design is similar to the open-pinned phase CCD described in [4] where the channel is inverted during the integration time. Instead of integrating charge under the P-type implant, we integrate charge under the electrode with an inverted surface. During the integration time, the entire surface is pinned with a large concentration of holes provided by the channel stops, which reduces the dark current at the interface.

An image is captured by integrating photocharge at each electrode or at every other electrode for higher well capacity. The integration begins by depleting the CCDs of charge via transfer to the upper diffusion V0. During integration, the pixel array electrodes are held at an intermediate voltage. At the end of integration, the accumulated charge is ripple transferred row-by-row to the storage array and then into the H-CCD one pixel at a time until every pixel has been double sampled at the floating diffusion and buffered by the source follower transistor.

Simulation and Measurement Results

Simulated potential diagrams along the channel (wherever the max potential occurs) for several phases are shown for all 3 designs in Fig. 14-16. Single electrode charge confinement is achieved in the surface-channel device due to the barriers created by the poly gap spacing, whereas it is achieved in the buried-channel device due to the induced pockets. The pinned phase design uses the self-aligned P-type implants as barriers to confine the charge. Although the surface potential is pinned to the channel stop potential, the depleted channel under the electrode remains at a higher potential. With sufficient gate voltage, each of the designs overcome the pocket or barrier that creates the confinement and charge is transferred away from one region and then packed again at single electrode pitch into another.

Confining charge at every electrode is made possible by using ripple charge transfer. Since we build distributed sub-arrays at the stack height scale, the overhead of employing ripple charge transfer is minimal. One drawback of the single electrode charge confinement is the reduced well capacity of about 500e-. We show that we can boost the well capacity by an order of magnitude by running in an interlaced mode where every other electrode induces a large barrier to confine more charge. By patterning the polysilicon at half the channel stop pitch, we could implement this method of operation at our current pixel scale without interleaving. At the current process node, this would require pre-doping the polysilicon.

Charge transfer efficiency is measured highest for the surface-channel device at just above 99.9%, whereas the buried-channel device has to be carefully tuned for this level of performance. When the devices show comparable CTE performance, the surface-channel also shows a slightly lower dark current than the buried-channel device. We also fabricated the surface-channel device with P-type channel stops and found that the CTE degrades. When the surface channel electrodes are first accumulated with holes, the CTE drops to as low as 85%, whereas the buried-channel device does not degrade under this condition. Although we can measure the CTE just after attracting the holes to the surface, we cannot operate the buried-channel device in this way during the integration period because the charge confinement region is eliminated as the surface is pinned. Therefore, the buried-channel device offers little to no benefit over the surface-channel device in terms of dark current performance. For this reason, we implemented the pinned phase buried-channel device that uses an extra implant between each electrode. This allows the surface to be inverted during integration and yet still contain the barrier necessary for charge confinement. The barrier potential relative to the channel potential under the electrode is shown in Fig. 17. The applied electrode voltages for V2 and V3 are labeled for each case. During the integration cycle, we need the potential under the electrode to be higher than the barrier potential in order to confine the electrons at the electrode. We also require that the surface potential be low enough to substantially increase the hole concentration. Since the inter-electrode implants are of P-type dopant, their potentials are lower than the buried channel under the electrodes even when the electrodes are low enough to pin the surface. This is the case when all electrodes are held at -1V. We are able to manipulate the barrier potential by increasing the potential of the adjacent electrode. When V3 is set to 3V, the barrier at V2 becomes substantially lower than the potential under V2, which causes the charge to transfer from one electrode to the next.

The conversion gain for the 0.5 μm pixel is 193μV/e- and 165μV/e- for the 0.7 μm pixel. There is no significant gain difference between the 3 types of CCDs because the readout transistors are identical. Despite the use of poly electrodes, the QE is reasonable for short wavelengths as shown in Fig. 18. This is due to the thin the poly layer and the open space in between each electrode. The dark current is about 35e-/sec for both the surface and buried-channel devices (See Fig. 19). The dark current improves by a factor of 15 for the pinned phase device. When operating in the pinned phase mode, the well capacity cannot be adjusted once the surface is pinned. We used a 4-way split on the n-channel doping profile in order to obtain a reasonable range of performance. Only the lower dopant levels were successful, which may demonstrate some limitations in the achievable well capacity with this approach.

Acknowledgment

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References

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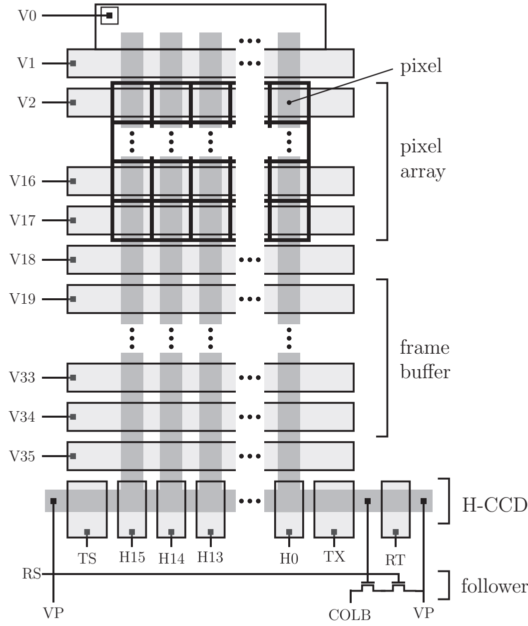

Fig. 1. FT-CCD schematic showing the pixel array, frame buffer, H-CCD and follower readout.

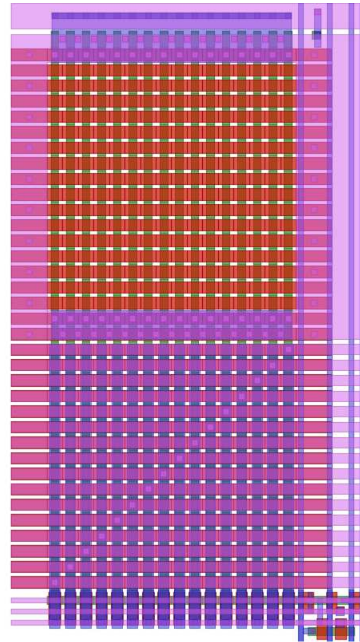

Fig. 2. CAD layout of the 16 × 16 FT-CCD.

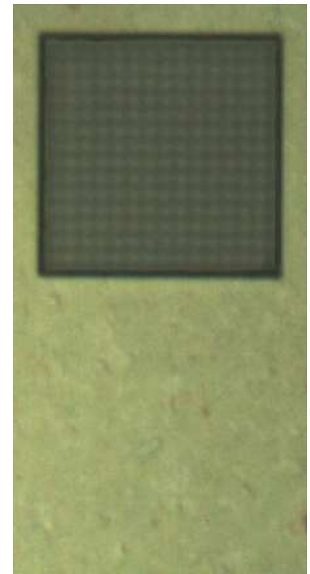

Fig. 3. Photomicrograph of a fabricated 16 × 16 FT-CCD. Two photos are combined to simultaneously focus on the pixels and the top metal.

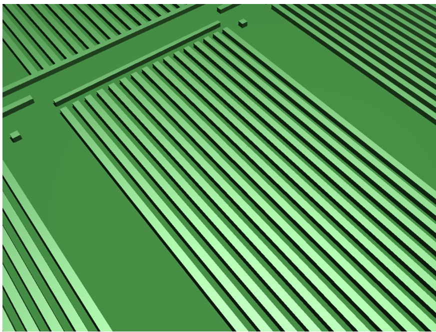

Fig. 4. Channel and channel stops for the FT-CCD.

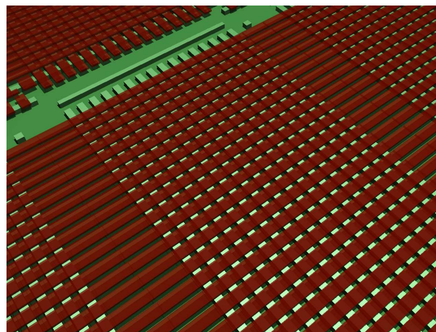

Fig. 5. Placement of the polysilicon electrodes.

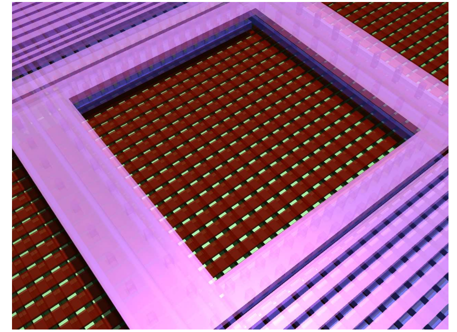

Fig. 6. Metal routing and isolation between arrays.

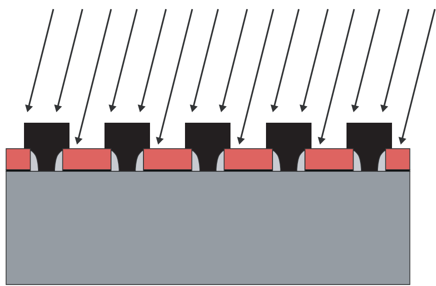

Fig. 7. Method for doping the polysilicon such that the channel region is protected.

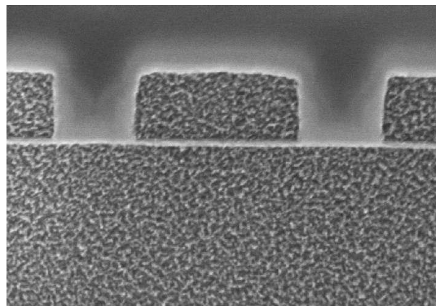

Fig. 8. Cross-section of the surface-channel CCD along the channel.

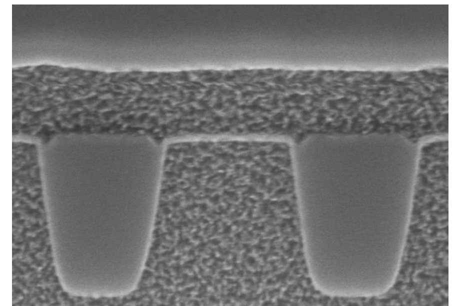

Fig. 9. Cross-section of the surface-channel CCD against the channel stops.

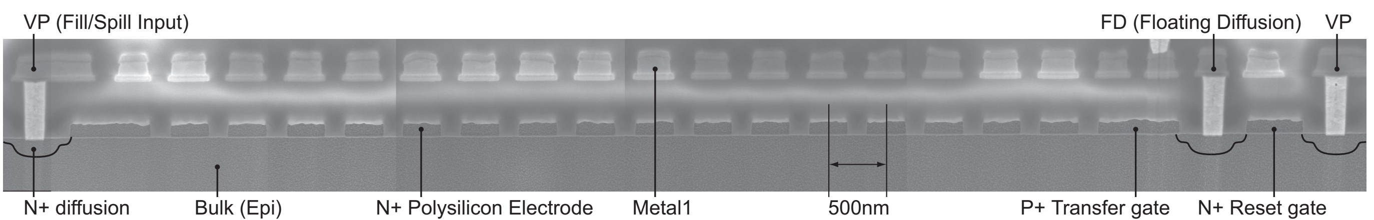

Fig. 10. SEM of 16-stage H-CCD showing fill/spill input for electrical testing, floating diffusion for output charge-to-voltage conversion, and the reset gate.

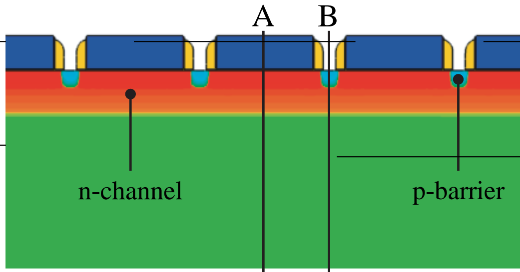

Fig. 11. Design of the pinned phase buried-channel CCD showing P+ electrodes with n-type channel against section A and self-aligned P-type barriers against section B.

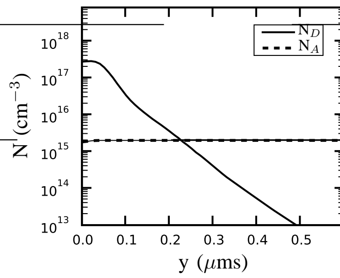

Fig. 12. Simulated doping profile along cross-section A.

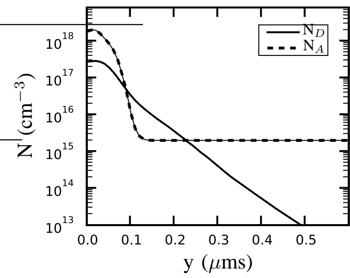

Fig. 13. Simulated doping profile along cross-section B.

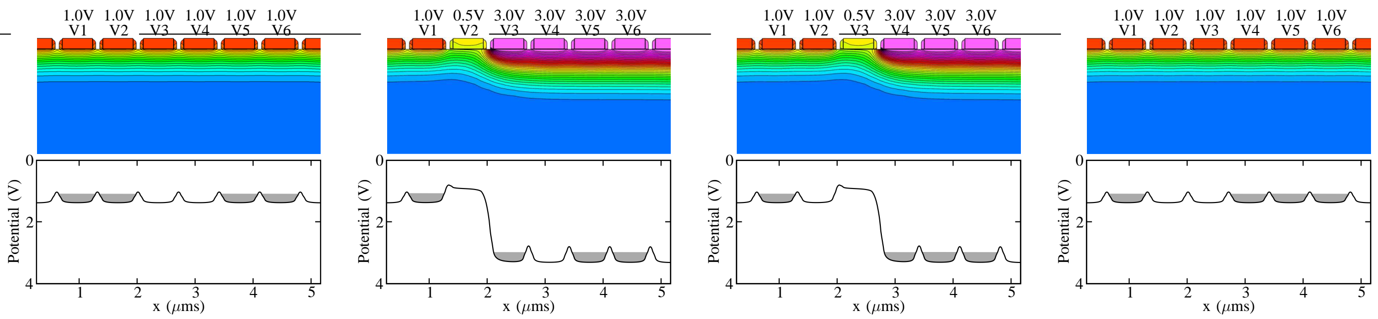

Fig. 14. Potential diagrams for the surface-channel CCDs with single electrode charge confinement during ripple charge transfer.

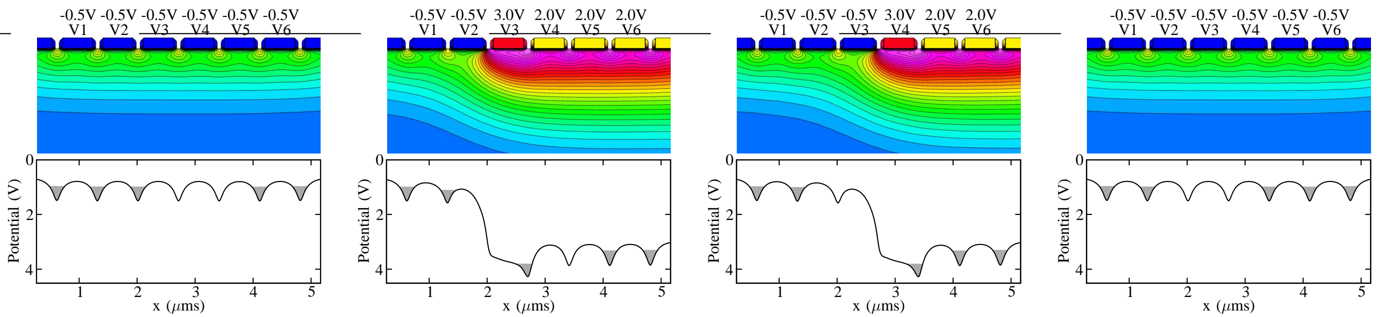

Fig. 15. Potential diagrams for the buried-channel CCDs with single electrode charge confinement during ripple charge transfer.

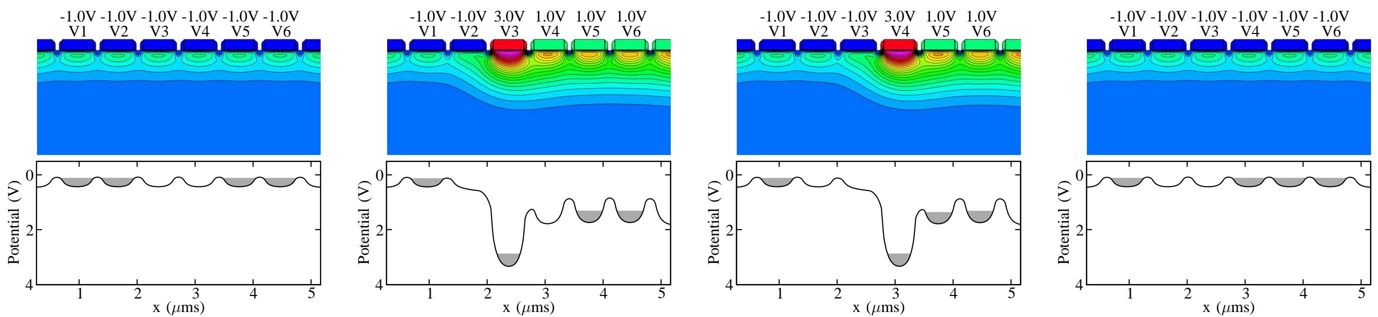

Fig. 16. Potential diagrams for the pinned phase buried-channel CCDs with single electrode charge confinement during ripple charge transfer.

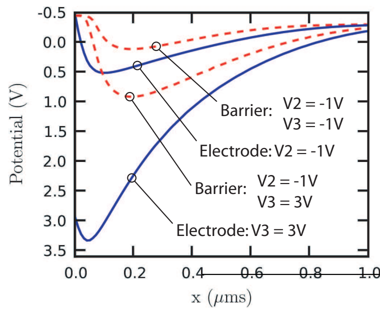

Fig. 17. Pinned phase diagram showing the barrier potentials relative to the potentials under the electrode region.

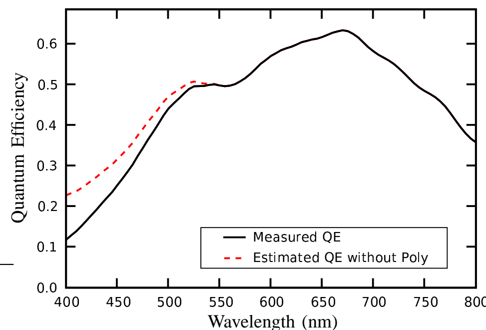

Fig. 18. Measured QE for the buried-channel CCD.

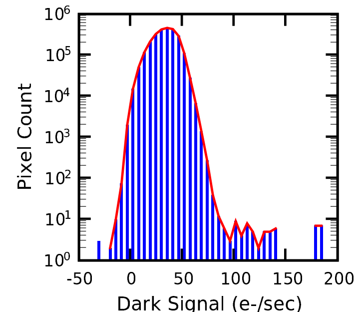

Fig. 19. Dark signal distribution for the buried-channel CCD at RT.