Backside Illuminated Image Sensors manufactured with Gradated Double Epitaxial Layers: an Application to a High-speed High-sensitivity Image Sensor

By T. G. Etoh[a)b)], T. Hayashida[b)], H. Maruyama[b)], T. Arai[b)], N. Uchiyama[c)] and T. Sakamoto[c)]

***Abstract*—A new technology is presented to manufacture functionable backside illuminated image sensors. The sensors are made by a process using wafers with thick n and p double epitaxial layers with gradated concentration profiles. Technical problems associated with the process are listed up. Their countermeasures were proposed and tested. The technology was applied to develop an ultra-high-speed and ultra-high-sensitive image sensor. A chip for fundamental test of the image sensor has been manufactured and evaluated. The maximum frame rate of the test chip is 250 kfps for the pixel count of 489x400 pixels and the dynamic range of 10 bits. An image with the signal level of 4.9e- can be detected on the noise floor of 7.7e-.**

***Index Terms*—backside illuminated, image sensor, multi epitaxial layers, gradated epitaxial layers, high speed, high sensitivity**

I. Introduction

IN 1991, a high-speed video camera of 4,500 fps was developed by Etoh[1)]. The highest frame rate in the world at the time was supported by the parallel and partial readout scheme. In 1993, he did a comprehensive questionnaire survey in Japan to find out user's requirements for the high-speed video cameras. The survey was repeated in 2000. Fig. 1 shows a result on the frame rate, which is summarized as follows[2)]:

(1) In 1993, the most frequent applications lie in the frame rate of 1 kfps to 10 kfps.
(2) Portion of applications requiring the frame rate higher than 1 Mfps is about 20%.
(3) The requirement for the frame rate increased by about ten times during the seven years between the two surveys.

In 2001, the authors developed a video camera operating at 1 Mfps at the maximum frame rate[3), 4)]. The color version was developed by NHK[5)].

The ultra-high frame rate was achieved by means of a special structure of a CCD imager, "An In-situ Storage Image Sensor (ISIS)" with slanted linear CCD storage, invented by Etoh and Mutoh[6)]. The structure is explained in the section II.

Immediately after the video cameras of 1 Mfps, we applied them to bioscience and nano-scale-science by attaching them to a fluorescence microscope, a transmission electron microscope, etc. The trials failed and disclosed further requirements of users for a video camera with ultra-high sensitivity as well as the ultra-high frame rate.

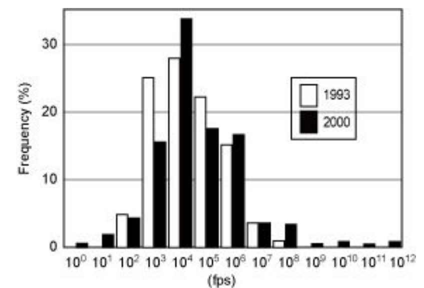


Fig. 1 User's requirement for frame rate (From questionnaires in 1993 and 2000)

In 2004, a new project "Development of Ultra-high-speed Bionanoscope" started with financial support of the Japanese government to develop a video camera with the frame rate up to 10 Mfps and the sensitivity to incident light of less than ten photons per pixel. The very high frame rate and sensitivity are respectively supported by the ISIS structure and a combinatory use of three existing technologies for high sensitivity; backside illumination, cooling and multi-step impact ionization, which was invented by Hynecek[7)] as CCM and currently widely applied in bio-science as EM-CCD.

To integrate these technologies, a new sensor technology "Backside-Illuminated Image Sensor on Double Epitaxial Layers with Gradated Concentration Profiles" was developed. It serves to develop backside illuminated image sensors with various useful functions, including the ultra-high frame rate, in addition to high sensitivity inherent to backside illuminated image sensors.

This paper presents advantages of and problems associated with the new technology, employing the ultra-high speed and ultra-high sensitivity image sensor as an application example.

In this paper, FSI and BSI image sensors stand for "Front-side Illuminated" and "Backside Illuminated" image sensors, respectively. Therefore, the example application sensor is called BSI-ISIS.

II. An Example Structere: BSI-ISIS

A. *Configuration*

Fig. 2 depicts the plane structure of the BSI-ISIS, which is installed on the front side. Fig. 3 and Fig. 4 show a cross section along A-A' line in Fig. 2, and an example of the potential profile with a path of an electron generated near the backside.

T. Goji Etoh is with Kinki University, Higashi-Osaka, 577-8502 Japan.
Tel +81-72-928-3130 email best2010@civileng.kindai.ac.jp
H. Maruyama, T. Hayashida and T. Arai are with NHK, 1-10-11 Kinuta, Setagaya, Tokyo, 157-8510 JAPAN
N. Uchiyama and T. Sakamoto are with Hamamatsu Photonics, 314-5 Shimo-Kamimasu, Iwata, Shizuoka, 438-0194 JAPAN

B. Cross-sectional Structure

In Fig. 3, an incident photon generates an electron-hole pair in the thick p- generation layer. The electron travels vertically in the generation layer to the n- collection layer, horizontally in the collection layer, and, again, vertically to the n+ buried channel under the collection gate on the front side to make a signal charge packet. The charge packet is transferred on an n+ CCD channel, which extends linearly in the orthogonal direction to the paper in the p-well. In Fig. 2, the CCD channel extends in a slightly slanted direction.

The CCD channel part and the collection gate part form an npnp and an np structures, respectively.

The configuration serves for the following advantageous functions:

(1) To prevent incident photons from directly reaching the memory CCD to generate additional electrons
(2) To prevent signal electrons generated in the generation layer from migrating to the memory CCD,
(3) To deplete the layers all the way along the path of the signal electron
(4) To decrease the reverse bias voltage applied to the backside of the sensor

C. Plane Structure

In Fig. 2, a charge packet is transferred from the collection gate to the memory CCD channel, carried downward and drained from the drain at the end of the CCD channel. Each slanted linear CCD serves as the memory for each pixel. The simultaneous parallel recording operation at all pixels realizes the ultimate high frame rate. The drain allows continuous overwriting recording during image capturing operation. When occurrence of the target event is detected, the overwriting operation is stopped, and, then, the image signals stored in the CCD memories inside the image sensor are slowly read out to a buffer memory outside the sensor. The overwriting mechanism is essential for ultra-high-speed imaging to ease synchronization of image capturing timing with occurrence of a target event.

The CCM is installed between the HCCD and the output amplifier.

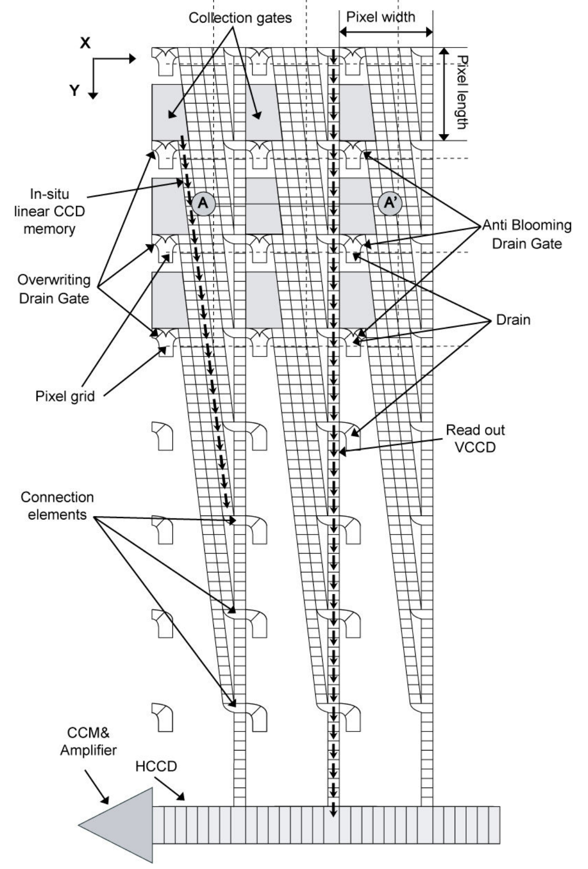


Fig. 2 Plane structure of BSI-ISIS on the front side

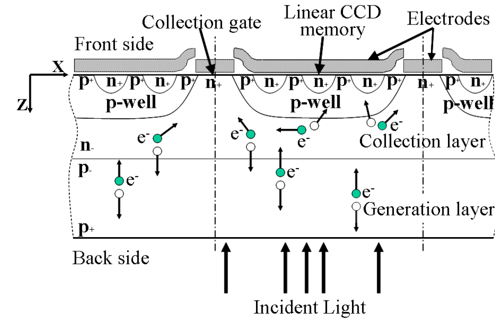


Fig. 3 Cross section structure of BSI-ISIS: A-A' section of Fig. 2

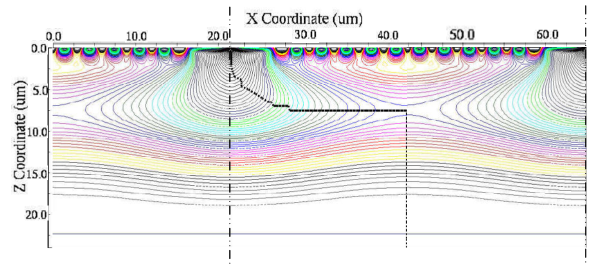


Fig. 4 Examples of a potential profile and an electron path

III. Double Epitaxial Layers with Gradated Concentration Profiles

A. Structure

To create the special doping profile shown in Fig. 3, a dedicated wafer with double n and p epitaxial layers was developed. The features of the wafer are summarized as follows:

(1) On a p+ substrate wafer, a p- epitaxial layer and, then, an n- epitaxial layer are overlaid.
(2) The concentrations of the epitaxial layers are low: for example, p is 5×10^{13} cm^{-3} ; n is 2×10^{14} cm^{-3}to 3×10^{14} cm^{-3}.
(3) They are thick: for example, the p layer is 20 um and the n layer is 10 um; the total thickness is 30 um.
(4) The concentrations are gradated.

In the n epitaxial layer, the p well is formed and the CCD channels are created in it by injection of impurity ions from the

front surface. The thickness of 30 um is sufficient to prevent red light from reaching the surface CCD memory.

Fig. 5 shows an example of the concentration profile of the special double-epi- wafer.

B. Advantages

The structure provides significant advantages in addition to those inherent to standard BSI imagers:

(1) Various useful functions can be installed in the p-well, avoiding penetration of incident light to the p-well and migration of electrons by diffusion into the p-well.
(2) Existing designs of FSI imagers made for standard n-wafers are easily convertible to the BSI imagers.
(3) Lower reverse bias voltage applied to the backside.
(4) Easy handling of thinned chips.
(5) No reflection of light by metals placed on the front side.
(6) High sensitivity for near-infrared and soft X rays.

For example, installation of memory cells in each pixel realizes ultra-high-speed imaging, as the BSI-ISIS utilizes. Pixel-based parallel processing units provide very fast automatic tracking function. An ADC in each pixel makes possible a stacked image sensor with memory chip directly attached to the front side of the image sensor chip. A range sensor sensitive to near IR is another application. Even to avoid image distortion of a moving target at high speed, at least one memory element is to be installed in the p-well.

The conversion to BSI imagers is made by making an n-type vertical electron path in the p-well and placing an electrode on the surface to create a collection gate in each pixel.

The gradated concentration profiles of double epi-layers serve for whole-layer depletion with lower reverse bias voltage.

The thickness more than 30 um enables handling of small chips with no pasted carrier to increase stiffness, except during backside thinning. Larger chips require thickness of 50-100 um, and, thus, a double-epi-wafer with much lower concentration.

No incident light reaches metals placed on the front surface, while the reflection causes spatial cross-talk for thin BSI imagers.

Near-infrared imaging is a common tool for security monitoring, which has significant business potential, especially when it is used with combination of near-infrared LED illumination.

Naturally, image sensors made with the thick double-epi-wafer have the advantageous features of common BSI imagers as well as those listed up above:

(1) Higher fill factor and higher quantum efficiency
(2) Higher freedom in the design of circuitry on the front side without care for losing the fill factor and uniformity among the pixel designs.
(3) Further functionality by stacking a supporting IC on the front side, which also serves for compactness.
(4) Imaging with a wider spectrum range of light, or electromagnetic rays with various functional coating on the backside, including UV rays.

For example, the frame rate can be easily increased with wide and stacked metal wires almost freely placed on the front side. For more flexibility and yet organized layout, the pixel-block-based design is commonly employed.

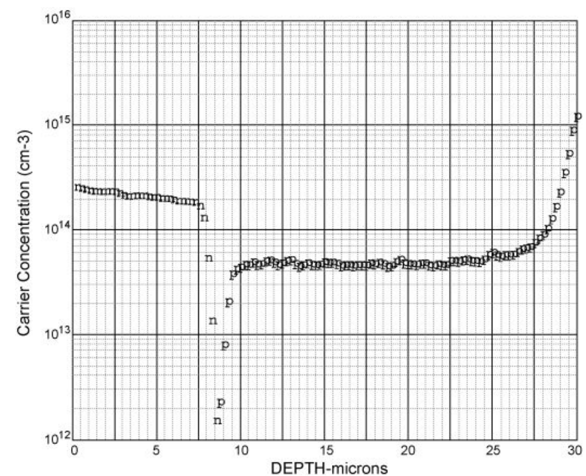


Fig. 5 An examples of a concentration profile of gradated double epitaxial layers: Measurement result by SR

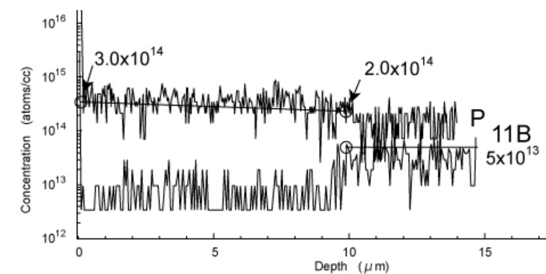


Fig. 6 An examples of a concentration profile of gradated double epitaxial layers: Measurement result by SIMS

C. Problems and Countermeasures

1) Problems

We faced some problems in the course of development of the BSI imager with the double-epi-wafer as follows:

(1) Large leak current generating along the np junction at the diced edge of the chip.
(2) Insufficient accuracy of concentration measurement
(3) Spatial cross talk due to oblique incident light at the outer photoreceptive area
(4) Voltage supply to and hole drain from the backside

The latter two problems are not serious. For example, the problem of oblique incident light may be solved by proper combination of a telecentric lens system and an on-chip micro lens array.

Hereafter, the former two problems are discussed in detail with the countermeasures.

2) Leak Current from Junction at Dicing Edge

Mechanical dicing of the double-epi-wafer exposes an np junction on the rough dicing edge which causes strong leak current. Fig. 9(a) shown later is an image of a beam chopper taken with a test sensor of the BI-ISIS in room temperature without cooling.

The dark stripe along the left edge is due to the leak current. By cooling, the dark stripe seemingly disappears. However, the noise level of the left edge is still significantly large.

As a countermeasure to the leakage, we applied stealth dicing instead of common mechanical dicing. The stealth dicing, SD,

was developed by Hamamatsu Photonics[8), 9)]. The basic principle is explained in Fig. 7.

(1) Step 1 Laser process: Laser beam energy of transmissible wavelength is absorbed only around focal point in the wafer by temperature dependence of absorption coefficient of the wafer, which locally creates fine crack s . Repeating the laser shots along the dicing line, a linear fructured zone connecting the fine cracks is created in the cross section, keeping the upper and the lower layers of the wafer intact.

(2) Step 2 Separation process: The wafer is mounted on an adhesive elastic tape, which is expanded to apply a tensile stress to the wafer; then, the internal cracks progress towards both surfaces of the wafer to separate it to individual chips.

The stealth dicing provides high quality dicing and clean process environment, characterized by the following “4 No s”: (1) No crack on the diced surface except the fractured zone, (2) No chipping dust to the clean room, (3) No kerf loss area, (4) No water (completely dry process)

The stealth dicing is applied to the test chip, resulting in a dramatic improvement. The leak current decreased 1/100 to 1/1,000 of that generated when the mechanical dicing is applied as shown in Fig. 8.

Laser annealing after Boron ion injection to the stealth dicing surface further decreased the leakage to 1/10. Detailed report will be presented elsewhere.

3) Concentration Control

Simulation shows lower concentration improves some of the performance indices of the sensor. The reasons are as follows:

(1) The chip can be thicker, which eases handling the thinned chip and widens the range of usable wave lengths.

(2)The hole accumulation layer becomes thinner, which increases the quantum efficiency and decreases the spatial cross talk.

(3) The mobility of electrons becomes higher, which suggests further increase of the frame rate.

Due to the accuracy limitation of the concentration measurement, in the current design, a slightly higher value than 10^{14} cm^{-3} and the middle of 10^{13} cm^{-3} are respectively employed for the n and the p epitaxial layers.

Hereafter, accuracy of concentration measurement is discussed based on our experience.

To measure varying concentration in the depth direction, surface concentration measurement technologies are applicable, such as SR and SIMS. If the concentration is not very low, FTIR is capable of measuring the depth of the pn junction.

The SR measurement is most commonly used, because of the simplicity and relatively high accuracy. However, the SR provides a smaller value for the depth of the np junction. When the measurement surface reaches close to the junction, the resistivity increases due to the existence of the depletion layer, while, immediately after passing through the junction, the depletion layer disappears to give normal measurement results.

Accuracy of SIMS significantly drops for the concentration below 10^{15} cm^{-3}, depending on the molecule species.

Fig. 5 and Fig. 6 respectively show examples of the SR and SIMS measurements. The targets values of the test wafer are as follows:

(1) The junction depth: 10.0 um

(2) The n layer concentration is 3.0×10^{14} cm^{-3} at the front surface and 2.0×10^{14} cm^{-3} at the junction; the p layer concentration is constant at 5×10^{13} cm^{-3}

The SR measurement result is summarized as follows:

(1) The concentrations of both n and p layers are close to the target values.

(2) The junction is located at 8.5 um, which is 1.5 um shallower than the target value.

The result of the SIMS analysis is summarized as follows:

(1) The concentration data scatter, far from the target values.

(2) The phosphor ion concentration for the n layer decreases around at 10 um from the surface; the boron ion concentration for the p layer increases at 10 um. The result suggests that the junction depth is about 10 um.

FTIR analysis to measure the junction depth failed due to the low concentration.

Consequently, a combinative use of SR and SIMS is recommended at the current state: SR for concentration measurement; SIMS for measurement of the junction depth.

However, the accuracy is too low. Further improvement of the measurement technology is expected.

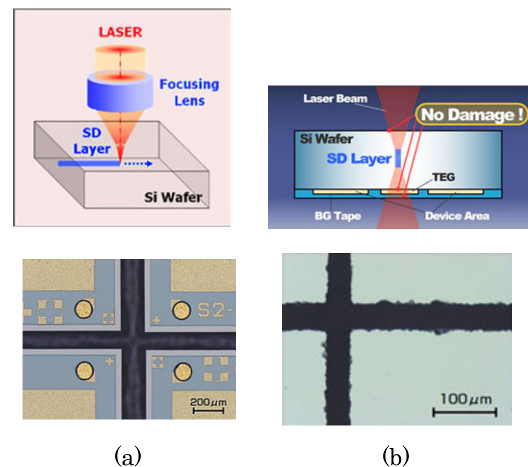


Fig. 7 Conceptual explanation of Stealth Dicing
(a)Stealth dicing (after stretching) (b) Mechanical Dicing

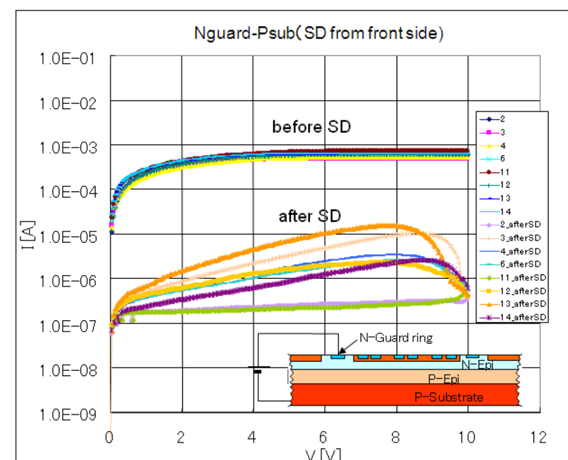


Fig. 8 Leak current vs. applied voltage
Decrease of leak current by means of Stealth Dicing

IV. APPLICATION OF WAFER WITH GRADATED DOUBLE EPITAXIAL LAYERS TO BSI-ISIS

A. *Performance of the Test Sensor ISIS-V12*

An ultra-high-speed and ultra-high-sensitivity image sensor is under development by creating the structure of the BSI-ISIS on the wafer with the double epitaxial layers with gradated concentration. The test sensor "ISIS-V12 (version 12)" has been manufactured and tested. The prototype is under process.

Table 1 shows performance of the test sensor. The sensor is cooled down to -40 degree C. The charge handling capacity is 10,000 e-. The total noise level of the system of the evaluation camera mounting the test sensor is around 9 e-, which may be mainly due to noise from our hand-made test camera system. Up to 250 kfps, the SN ratio remains constant at 10 bits.

B. *Comparison of Sensitivity of Front-side and Backside Illuminated ISISes*

The simplest way to show improvement of the performance, including an increase of sensitivity, is comparison of the test sensor of the BSI-ISIS with the existing FSI-ISIS. Fig. 9(a) and (b) show two images taken by the two cameras mounting a FSI-ISIS and a BSI-ISIS at the frame rate of 1 kfps and 8 kfps, respectively, in room temperature. Other imaging conditions are the same. The CCM of the BSI-ISIS is not activated.

Although the image of the BSI-ISIS was taken at eight-time higher frame rate, it is brighter than that of the FSI-ISIS, which proves that the BSI-ISIS without cooling and the CCM has about ten-time higher sensitivity than the existing FSI-ISIS.

The FSI-ISIS is equipped with a memory area in each pixel which is covered by a metal light shield. Therefore, the fill factor is very low, about 13%. The pixel area of the FSI-ISIS is 3.22 time larger than that of the BSI-ISIS. Considering these numbers, the QE of the BSI-ISIS is about three-time higher than that of the FSI-ISIS.

C. *Efficiency of CCM*

The CCM is a very efficient CCD-specific amplification method, utilizing a multi-step impact ionization process. In each CCD element, high electric field created by a large voltage difference ΔV_{CCM} of two adjacent electrodes accelerates electrons to generate a very small number of the secondary electrons. By repeating this independent impact ionization process, signals are amplified with less increasing additional random noise associated with the process.

Fig. 10 and Table 2 show ΔV_{CCM} versus the average, S_{NOM}, of output signals from pixels of the test sensor in a rectangular area A shown in Fig. 9(a). S_{NOM} is a nominal average signal level, since it is a sum of the image signal S_{NET} created by the very weak incident light and the noise N_{NET}, mainly consisting of dark current, readout noise and camera system noises.

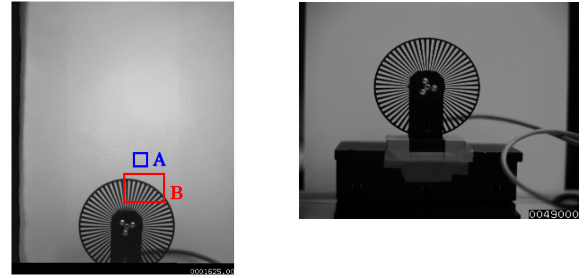
The imaging condition is also described in the tables. Incident light to the sensor is very weak and further reduced by attaching four ND filters with reduction factors of 1/8, 1/4, 1/4 and 1/2 in front of the lens of the test camera.

In Table II, the standard deviation N_{NOM}, the nominal SN ratios SNR_{NOM} (= S_{NOM}/N_{NOM}) and the amplification factors F_{AMP} (= S_{NOM}/S_{oNOM}) are also tabulated, where S_{oNOM} is the nominal average signal level without the CCM amplification.

TABLE I

SPECIFICATION OF THE TEST SENSOR OF THE BI-ISIS (ISIS-V12) AND THE FI-ISIS (ISIS-V2)

	ISIS-V12	ISIS-V2
Frame Rate	250,000 fps (1,000,000 fps)	1,000,000 fps
Pixel Count	489 x 400 (=195,600)	312x260 (=81,120)
Pixel Size	43.2 x 43.2 microns^2	66.3x66.3 micron^2
Size of CCD Element	3.0 x 3.6 micron^2	5.1x5.1 micron^2
Fill Factor	100% (1866 micron^2)	13% (580 microns^2)
Number of Frames	117 frames	103 frames
Transfer Scheme	Four-phase transfer	Four-phase transfer
Operating Temp.	-40 degree C	> 5 degree C
Sensitive Wavelength	450 nm ~ 650 nm	450 nm ~ 700 nm
Overwriting Operation	Installed	Installed
CCM	Installed	Not installed



(a) BI-ISIS 8,000fps (200 kpixels) (b) FI-ISIS 1,000fps (80 kpixels)

Fig. 9 Comparison of brightness of BI-ISIS and FI-ISIS. Temperature: 25^{0}C; Lens: Nikkor 50mm; Iris: F1.2; Illumination: 300lx

From these figures and tables, it is observed that:

(1) The amplification factor F_{AMP} of the CCM sharply increases for ΔV_{CCM} > 26 V, which reaches to about 300 times for ΔV_{CCM} = 29 V.

(2) When the CCM is applied, SNR_{NOM} increases from 0.8 and exceeds 2.0 for ΔV_{CCM}> 27 V.

Fig. 11 shows example images for these imaging conditions. The object is the upper-right quarter part of the laser-beam chopper shown with B in Fig. 9(a).

The net signal and net noise levels, S_{NET} and N_{NET}, can be estimated for the imaging condition. The nominal output signal S_{NOM} is measured for increased incident light by detaching the ND filters one by one. For example, when only one 1/8-ND filter is attached, by detaching three ND filters of 1/4, 1/4 and 1/2, the net signal level S_{NET} is increased by 32 times, keeping the noise level N_{NET} constant. For the condition, the S_{NOM} is increased to 163.4 e-, while the value with all four ND filters is S_{0NOM} = 12.6 e-, as shown in Table 2. Therefore, the following approximated relationships can be assumed:

$S_{NET} + N_{NET}$ = 12.6 e- ; $32S_{NET} + N_{NET}$ = 163.4 e-

By solving the equations, S_{NET} = 4.9 e-, and N_{NET} = 7.7 e-.

The value of N_{NET}; 7.7 e-, is reasonable, since it is close to the

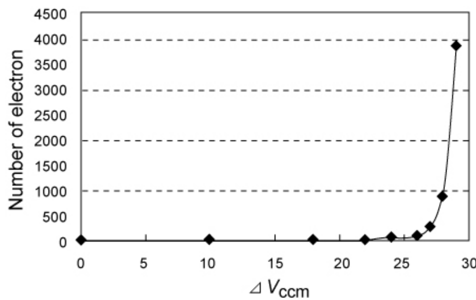


Fig. 10 Average of output signal level vs ΔV_{CCM}. Frame rate: 8 kfps; Temperature: -40^{0}C

AMPLIFICATION OF VERY WEAK SIGNALS BY MEANS OF CCM

FRAME RATE: 8KFPS, TEMPERATURE: -40°C

CCM	Amplifica	Average	St. Dev.	SNR
ΔV_{CCM}(V)	F_{AMP}	$S_{NOM}(e^-)$	$N_{NOM}(e^-)$	SNR_{NOM}
0.0-10.0	1.0	12.6	15.0	0.8
18.0	1.1	13.6	15.6	0.9
22.0	1.6	19.8	18.8	1.1
24.0	2.8	35.0	25.8	1.4
26.0	7.5	94.8	65.4	1.4
27.0	22.7	286.4	145.0	**2.0**
28.0	69.9	880.2	398.8	**2.2**
29.0	309.2	3896.8	1711.0	**2.3**

total noise level with no incident light, 9 e-.

In Fig. 11, it is noticeable that the chopper with image signals of 4.9 e- embedded in the noise floor of 7.7 e- becomes recognizable by application of CCM with ΔV_{CCM} > 27 V, for which SNR_{NOM} > 2.0. On the other hand, the image is undetectable by a conventional amplifier.

V. CONCLUDING REMARKS

A structure of backside illuminated image sensors is presented. The circuitry is manufactured on the wafer with thick double epitaxial layers with low and gradated concentration. Large leak current is generated at the dicing edges of the sensor. Stealth dicing is a powerful tool to solve the problem. Further technical development is expected to accurately measure the low and gradated concentration. A test sensor of an ultra-high-speed and ultra-high-sensitivity image sensor was made by using the special wafer. The test chip proved that the sensor concept on the double-epi-wafer is promising to develop highly functional compact image sensors with high sensitivity.

A prototype image sensor is currently under process, which operates at 10 Mfps at the maximum frame rate and is capable of capturing images for incident light less than 10 photons per pixel.

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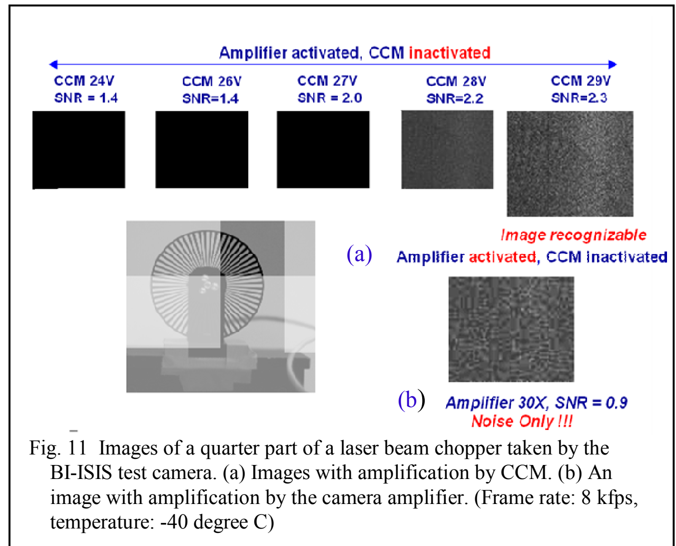

Fig. 11 Images of a quarter part of a laser beam chopper taken by the BI-ISIS test camera. (a) Images with amplification by CCM. (b) An image with amplification by the camera amplifier. (Frame rate: 8 kfps, temperature: -40 degree C)

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