

Comparison of Several Ramp Generator Designs For Column-Parallel Single Slope ADCs

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Abstract—Many CMOS image sensors now use column-parallel readout structure with single slope ADCs. Ramp generator in the ADCs is a critical building block since the performance of the ADCs depends a lot on the accuracy of the ramp signal. In this paper, we present several ramp generator architectures and compare their performance in terms of resolution, area, noise and reliability.

I. INTRODUCTION

CMOS image sensors have become very popular in mobile phones, notebook cameras, security and automotive applications. Especially in mobile phones, megapixel sensors have become the mainstream resolution, replacing VGA sized sensors. As sensor resolution increases, higher data conversion rates are required to maintain the same frame rate. To achieve low power and higher data conversion rate, many sensors employ single-slope column-parallel ADCs [1]-[3]. Compared to the global pipeline ADC approach, this approach can achieve lower read noise, and thus higher dynamic range, because of reduced bandwidth required in readout circuit for each column's ADC.

A critical building block in the single-slope column-parallel architecture is the ramp generator. Sensor noise, FPN, linearity, and yield characteristics depend greatly on the ramp generator design and specifications. First of all, because the ramp signal drives an ADC in every column, it needs to be immune to kickback noise from the ADC array. Second, because of the global distributed nature of the ramp signal, it can be a major source of supply noise induced row-wise noise. Third, any nonlinearity in the ramp is translated into the DNL and INL error of each ADC directly. The ramp generator must therefore have good driving capability, fast settling, good supply rejection, and excellent linearity.

Other considerations in the ramp generator design are its scalability to higher ADC resolution, and the ability to implement multiple knees in the ramp signal to reduce the conversion time [4]. This requires the ramp signal to have an accurate ratio between different slopes, or to have faster settling times with a high

speed clock. In this paper, we compare several ramp generator designs based on these requirements. In order to appreciate power, speed, and accuracy requirements for different ramp designs, we use a 5 MP (2592 x 1944), 15 fps sensor requiring a 10-bit resolution. As the signals from pixel array have to go through the CDS and column ADC circuits within around 30 μ s row-time, we will use 20 ns per 1 mV ramp step to achieve a 1 V ramp swing in 20 μ s. We further assume the ramp generator is driving a total of 40 pF column load to estimate the power and speed requirements for different ramp designs presented in Section III–VI.

II. OVERVIEW OF RAMP GENERATOR DESIGN

Various ramp generator design approaches can be found in the literatures [6]-[11]. In principle, these designs create a ramp waveform by progressively incrementing or decrementing a signal in voltage, current or charge domain. This is accomplished with a voltage DAC, current DAC or capacitive DAC, or with an integrator with either continuous or discrete time response. All of these designs require a master voltage or current reference to create the ramp steps. A typical system level block diagram of the ramp generator is shown in Fig. 1. To make a fair comparison between different ramp designs, we assume that the reference generation blocks (bandgap, voltage reference, current DAC) are the same for all of the ramp generator designs.

The ramp generator's power supply rejection ratio (PSRR) is determined by the PSRR of the reference generation block and that of the actual ramp circuit. The PSRR is critical because power supply induced ramp noise is a major source for image sensor's row-wise noise. To make the row-wise noise imperceptible, studies have shown it should be at least five times smaller than the read noise [5]. If the read noise of the readout chain is 1 mV_{rms}, this yields about 200 μ V_{rms}. To reach this level, the PSRR should be above 54 dB, assuming a supply noise of 100 mV_{rms}. Note that this PSRR specification should include not only the ramp generator, but also all the reference generation blocks depicted in Fig. 1. The more blocks are involved in the ramp generation path, the more power supply noise will likely to be introduced.

III. FLASH RESISTIVE DAC

The first ramp generator design we are discussing here is a flash DAC using resistor dividers. This architecture has been mentioned in [6], [7]. A simplified schematic is shown in Fig. 2. The step size of the ramp can be controlled by the tail currents through the switches G[0]-G[3]. The advantage of this approach is that it is guaranteed monotonic, and the slope of the ramp is not sensitive to supply and temperature variations, which means the row-wise noise of the sensor is low. During ADC operation, kickback noise from the column comparators can be very large. As such, a unity gain buffer is needed to isolate the ramp output from column comparator circuits. If the settling error requirement is no greater than 1/16 of the ramp step size, the buffer needs only settle to 4-bit accuracy. This leads to a unity gain bandwidth of about 22 MHz based on the sensor requirements assumed at the end of Section I. Since the unity gain bandwidth is g_m/C_L , assuming V_{dsat} of the input differential pair is about 150 mV, the total current of the buffer amplifier can be less than 1 mA. If the current running through the resistor ladder is about 0.2 mA, the total current consumption of this ramp generator is around 1.2 mA.

The disadvantage of this approach is that it is hard to scale when the resolution of ADC increases above 10-bit. This statement is true for both linear ramp and piecewise linear accelerated ramp, because more resistors are needed in the ladder which increases the size of the block. In addition, the linearity of the ramp is largely decided by resistor matching, which is usually around 10-bit. Thus, it is difficult to scale this ramp generator design to ADC resolution greater than 10-bit.

IV. CAPACITIVE DAC

The second approach is to use a capacitive DAC to generate the ramp signal [8], which is shown in Fig. 3. The top plates of the capacitor array are tied together as the ramp output signal. When the bottom plates of the capacitors are switched from V_l to V_h or V_h to V_l in succession, the voltage on the top plate ramps up or down depending on the difference between V_h and V_l . The advantage of this approach is that the kickback noise is small because the total capacitance from the capacitor array is much larger than the load from the comparators. As a result, generally no output buffer is needed at the ramp output. But this approach needs at least two other drivers; one is the clamp driver which drives the top plate of the capacitor array during reset time to set the starting voltage of the ramp. The other is a unity gain buffer for V_h driving the bottom plate of the capacitor array. V_l can be set to ground, so no driver is needed.

The clamp driver is relatively slow. If the total settling time of the clamp voltage is 2 μ s, in which 1.2 μ s is allocated for slewing, and the unity capacitor C in Fig. 3 is 250 fF for 10-bit ADC resolution, then the unity gain bandwidth of the driver is estimated to be around 1.4 MHz, and the total current consumption is less than 400 μ A. But the critical specification for the clamp driver is its supply rejection performance. It should be above 54 dB, as we calculated before, to reduce row-wise noise.

The design of the V_h driver is difficult due to the large capacitive load from the array and fast settling time. This driver has to be stable over a large range of loading condition, which is from 250 fF at the first step to over 100 pF at middle scale. And it needs to have enough bandwidth and slewing capability for all the loading conditions to settle in time. A single stage driver will need more than 30 mA to driver such a big load quickly. A class-AB driver can be used to reduce the quiescent current to below 3 mA. But compared with the resistive DAC, the total current consumption is still much higher. And scaling to higher resolution is also difficult because the capacitor array size has to be doubled with each additional bit, and the driver needs to consume even more power.

V. SWITCHED-CAPACITOR INTEGRATOR

The third approach is to use a switched-capacitor integrator to generate the ramp signal [9]. A simplified diagram is shown in Fig. 4. The sampling capacitor C_s of the integrator samples V_1 and V_2 at different clock phases. The difference between the two voltages is integrated on the feedback capacitor C_f at phase 2 of each clock cycle. The step of the ramp is then given by $C_s/C_f \cdot (V_1 - V_2)$. In this approach, the noise from the resistor ladder is scaled down by the gain of the integrator C_s/C_f , so it can be ignored when the gain of the integrator is much smaller than one. The ramp noise mainly comes from the integrator itself and its buffer. The advantage of this approach is that the step size and the resolution of the ramp are much easier to be changed compared to the first two approaches. And a differential type of ramp signal can also be generated using a switched-capacitor integrator [10]. With a differential ramp signal, common-mode noise can be rejected by the comparators in the column. However, the differential integrator needs a continuous common-mode feedback circuit with wide linear range. With reduced supply voltage levels, this becomes more and more difficult.

The main problem of this approach is that since the step size of the ramp is so small, and the sampling capacitor size is also very small due to the limitation of die size, the charge in the switch channels can be as

large as several percentage of the charge being transferred from the sampling capacitor to the feedback capacitor. As a result, the gain error caused by charge injection could be much higher than that caused by capacitor mismatch. Take 100 fF as the sampling capacitance. If the supply voltage is 2.8 V, V_1 is 1 V, V_2 is 2 V, V_{th} is 0.6 V, the switch size is $1 \mu\text{m}^2$, and C_{ox} is $5 \text{ fF}/\mu\text{m}^2$, then the total charge we intend to transfer is $C_s \cdot (V_2 - V_1) = 100 \text{ fC}$ while the channel charge in the switch transistor when sampling V_1 is $C_g \cdot (V_{dd} - V_1 - V_{th}) = 6 \text{ fC}$, which is about 6 % of the charge to be transferred. In this case, charge injection error can cause a gain error up to 6 %.

Furthermore, the charge injection is also supply and temperature dependent, which can cause more variations and nonlinearity in the ramp output. This situation will become worse when multi-slope accelerated ramp is used to increase the ADC resolution. When the ramp slope changes by varying the difference between V_2 and V_1 , the error caused by charge injection also changes. This makes the relative gain between the different segments of the ramp signal unpredictable. An additional feedback circuit to calibrate the ramp signal is needed for this approach. And DNL will likely be degraded because of calibration in that case.

VI. CONTINUOUS RAMP WITH CAPACITIVE TRANSIMPEDENCE AMPLIFIER (CTIA)

Fig. 5 shows a continuous ramp generator using a CTIA structure with constant current as input [11]. All the ramp generators discussed before have staircase type of responses. Their slopes are inversely proportional to the clock period, but the step sizes are independent of the clock speed. Thus, clock frequency variation and clock jitter do not affect the linearity or resolution of the ADC. However, for a continuous ramp generator, clock frequency variation and clock jitter not only affect the linearity and resolution of the ADC, but also affect the gain of the signal chain. In addition, the input current generated on-chip has a wide range with PVT variations. So a calibration of the ramp signal against the clock frequency is every critical. This calibration can be done in either analog domain or digital domain. The analog calibration is to run the ramp at fixed clock cycles and compare the output with a targeted voltage. The digital method is to run the ramp to a targeted analog voltage, and count the clock cycle to reach there. In both methods, the difference is then fed back to the input current DAC to adjust the current. To get some idea on the design variables, consider the case with a capacitor array (1024 capacitors with 100 fF) as the CTIA feedback. The slope of the ramp is $1 \text{ V}/(20 \text{ ns} \times 1024)$. So the input current can be calculated as $(1024 \times 100 \text{ fF}) \times$

$1 \text{ V}/(20 \text{ ns} \times 1024) = 5 \mu\text{A}$. This design is also vulnerable to kickback noise. So an output buffer is also needed.

The biggest advantage of this approach is its scalability with respect to frame rate. For higher frame rate, the clock frequency increases, and the ramp slope should be larger. To make the ramp runs faster in this case, one can simply reduce the size of the feedback capacitor. Thus, the area of the ramp generator becomes smaller. All the other discrete ramp generators which require small settling error will grow bigger when the clock is running faster.

Another advantage of the continuous ramp is that the companding mode ADC operation can be implemented simply by varying the clock speed for the ADC. For small signals, the ADC can be clocked faster to have higher resolution, whereas at higher signal levels, the ADC can be clocked slower to compress the output. We don't have to worry about the slope ratio matching as in the switched-capacitor integrator case.

VII. SUMMARY

We have discussed the most prominent features of several ramp generator architectures. In summary, the resistive DAC approach is easier to design and is less sensitive to PVT variations, but its resolution is limited by resistor matching and area. The capacitive DAC approach is less sensitive to kickback noise, but designing low power drivers to drive the bottom plate of the capacitor array is difficult. The integrator approach is more flexible and easier to scale than the others. But it is the most sensitive one to PVT variations. Additional calibration circuit is needed to correct the slope on the fly, with possible negative implications on the DNL performance of the ramp. Running faster also requires the amplifier to consume more power and area. The continuous ramp generator has the biggest advantage of scalability when the speed requirement increases. The companding mode ADC operation is also easy to be implemented. But the slope of the ramp needs to be constantly calibrated to compensate for PVT variation. More comparisons between these ramp generators that are not discussed in details are shown in Table I.

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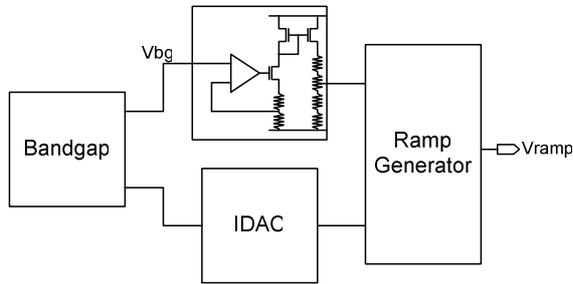


Fig. 1. System level block diagram of a ramp generator.

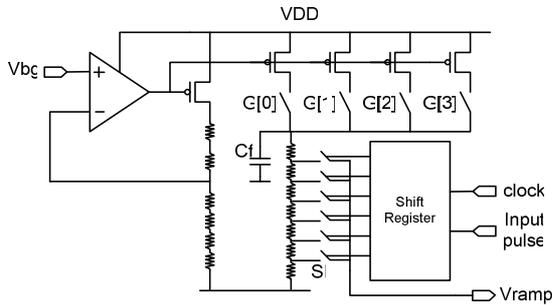


Fig. 2. Ramp generator using a resistive DAC.

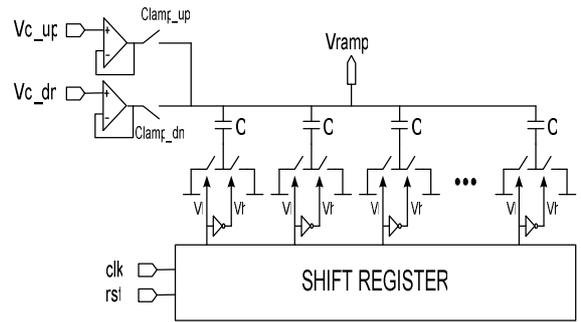


Fig. 3. Ramp generator using a capacitive DAC.

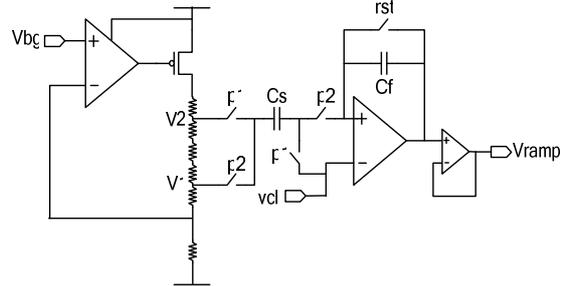


Fig. 4. Ramp generator using a switched-capacitor integrator.

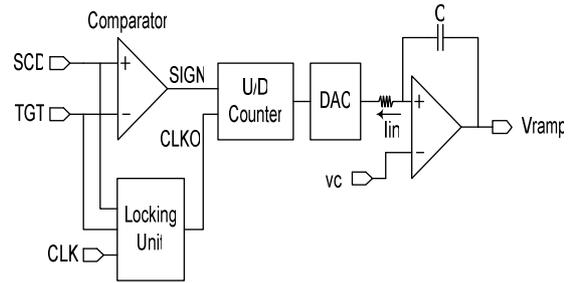


Fig. 5. Continuous ramp generator using a CTIA with auto-calibration.

TABLE I. Comparison of different ramp generators.

	RDAC	CDAC	SC Integrator	Differential SC Integrator	Continuous CTIA
Power	Low	High	Medium	High	Low
Area Changes as ADC resolution increases	Higher	Higher	Same	Same	Same
Area Changes as frame rate increases	Slighter higher	Much higher due to much larger bottom plate driver	Higher due to larger drivers	Higher due to larger drivers	Lower due to smaller capacitance
Supply Rejection	Medium	Low	Medium	Higher	Low
Linearity	Limited by resistor matching	Limited by capacitor matching	Depend on amp linearity range	Depend on amp and common mode range	High
Resolution	Low	Low	High	High	High
Nonlinear Function Implementation	Difficult	Difficult	Hard to control ratio between slopes	Hard to control ratio between slopes	Easy to implement by varying clock speed
Clock Synchronization	Easy	Easy	Easy	Easy	Hard