Ultrasmall digital image sensor for endoscopic applications

Martin Wäny*, Stephan Voltz, Fabio Gaspar, Lei Chen, AWAIBA Lda. Madeira Tecnopolo, 9020-105 Funchal, Maderia Portugal.

ABSTRACT

This paper presents a digital image sensor SOC featuring a total chip area (including dicing tolerances) of 0.34mm2 for endoscopic applications. Due to this extremely small form factor the sensor enables integration in endoscopes, guide wires and locater devices of less than 1mm outer diameter. The sensor embeds a pixel matrix of 10'000 pixels with a pitch of 3um x 3um covered with RGB filters in Bayer pattern. The sensor operates fully autonomous, controlled by an on chip ring oscillator and readout state machine, which controls integration AD conversion and data transmission, thus the sensor only requires 4 pin's for power supply and data communication. The sensor provides a frame rate of 40Frames per second over a LVDS serial data link. The endoscopic application requires that the sensor must work without any local power decoupling capacitances at the end of up to 2m cabling and be able to sustain data communication over the same wire length without deteriorating image quality. This has been achieved by implementation of a current mode successive approximation ADC and current steering LVDS data transmission. An band gap circuit with -40dB PSRR at the data frequency was implemented as on chip reference to improve robustness against power supply ringing due to the high series inductance of the long cables. The B&W versions of the sensor provides a conversion gain of 30DN/nJ/cm2 at 550nm with a read noise in dark of 1.2DN when operated at 2m cable. Using the photon transfer method according to EMVA1288 standard the full well capacity was determined to be 18ke-. According to our knowledge the presented work is the currently world smallest fully digital image sensor. The chip was designed along with an aspheric single surface lens to assemble on the chip without increasing the form factor. The extremely small form factor of the resulting camera permit's to provide visualization with much higher than state of the art spatial resolution in sub 1mm endoscopic applications, where so far only optical fiber bundles providing 1k – 3k image points could be used. In many applications, such as guide wires and locater devices the small form factor permits to implement visualization for the first time.

* waeny@awaiba.com phone +351 291 7253 124; fax +351 291 720 031; www.awaiba.com

1 INTRODUCTION

The presented work addresses visualization in the endoscopic field, mainly for minimally invasive surgery and diagnosis. Especially for procedures in minimal size cavities or to locations where minimal diameter cavities have to be passed for access. Standard endoscopic equipment with distal image sensor technology (chip on tip endoscopes) was limited to endoscope diameters superior to 1mm, especially when besides the imaging channel working channels have to be added in the endoscope. This limitation mainly arose due to the used CCD imaging technology which is limited to analogue signal transmission, and requires multiple control inputs for readout. Typically CMOS Image sensors for endoscopic applications target similar applications than earlier CCD's or explored the low power consumption [1-3] or lower cost [4-5] of CMOS image sensors. However target generally applications which allow for sensor dimensions above 1mm. The demonstrated CMOS sensor technology addresses procedures where smaller endoscope diameters are required, namely where the total scope diameters needs to be below 1mm. The requirement to reduce sensor size considerably below $1mm^2$ and enabling operation without any external components, called for size reduction of all components in the SOC sensors and high PSRR blocks. The reminder of this paper will address the design of the over all architecture and the most critical blocks in required to integrate the sensor in the target chip area and finally will give characterization results.

2 SENSOR ARCHITECTURE

2.1 Chip architecture

In order to minimize surface consumption the chip was designed to work with a single 1.8V supply only. This permits to use smaller real estate for ESD protection. For critical matching the 1.8V MOS devices provide better miss match performance per gate area compared to the 3.3V counterparts. However the single 1.8V operation limit's the available head room for analogue circuitry, especially in the on chip band gap reference but also the ADC and most importantly the pixel matrix. All blocks must be able to cope with significant power supply noise, since no off chip decoupling capacitors are available and the power supply wiring can be up to 2.5m for some endoscopic applications. Figure 1 gives a simulated plot of the power rails including the full chip consumption and a wire model for a 2.4m supply and data lines. In order to reduce the supply current surge, the main blocks were designed in current mode schemes with constant total

current consumption. (Current steering instead of current switching). Figure 2 shows the block diagram of the chip, which is strictly reduced to the minimal amount of blocks necessary for autonomous function.

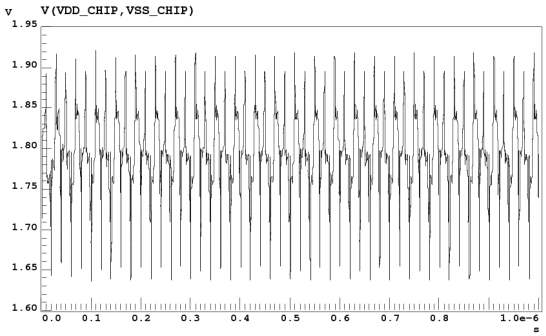

Fig. 1: *Simulation of the on chip power ripple due to 2.4m cabling.*

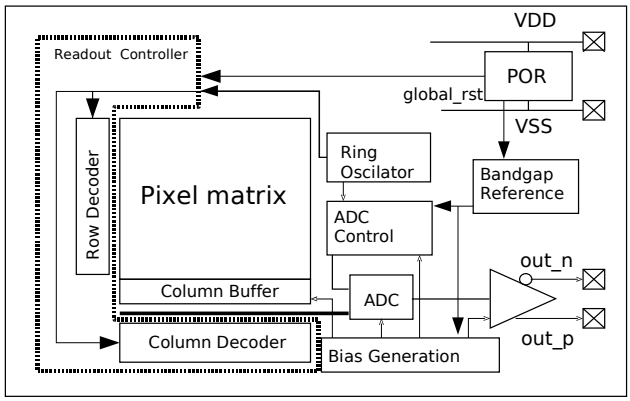

Fig. 2: *Chip block diagram.*

2.3 AD Converter

AD converters in image sensors are typically implemented as switched capacitor cyclic or pipelined architectures, [6] or more recently mainly as column parallel ADC's [7]. However both of these architectures are much too demanding for the available real estate of this sensor. For low cost wireless sensors [8;9] had presented charge redistribution based ADCs with only 0.05mm2 area at 100kHz resp. 0.034mm2 at 250kHz, which is in the target range of our adc of 90um x 250um, and 400kHz sampling rate. Due to the high expected ripple on the power supply the use of a capacitor based ADC was not preferred for noise coupling reasons. Therefore a current based SAR ADC was chosen. The reference current and a reference voltage is generated from the band gap voltage and multiplied by a DAC with 4 binary and 4 thermometer bits. In order to avoid ringing by changes in current consumption, the total current consumption of the IDAC is maintained constant, and the non used current is drained. A successive approximation register compares the sampled input signal with the programmable I-DAC voltage and adjusts in binary way. The block diagram of the 8bit SAR is shown in figure 3.

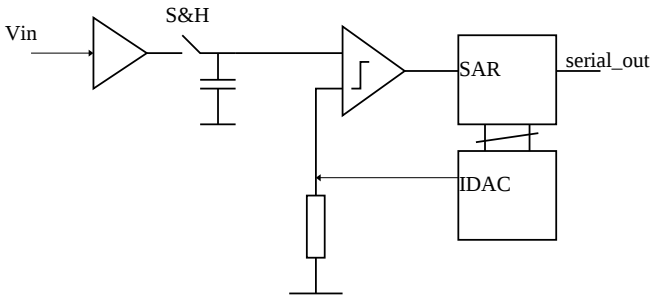

Fig.3: *Block Diagram of the semi current mode 8bit SAR-ADC*

The over all timing of the ADC is made such that the ADC produces an 8bit sample every 10 clocks. The SAR output is directly used as bit serial output stream to the LVDS driver. Therefore the SAR reset state and tracking phase of the S&H stage had to be aligned such that they provide a start and stop bit for the bit serial data communication. The ADC works at 400kS/s with a 4MHz frequency to support a frame rate of 40Fps. The comparator offset is not important in this architecture nor the absolute current reference offset, since both will only lead to an over all offset shift of the pixel values, however both of them have to be insensitive to variation of the supply voltage.

3 RESULTS

3.1 ADC performance

The ADC was implemented for test purpose in a separate test chip. The characterized DNL of the ADC is shown in figure 4. Due to a miss match slightly above estimation in the IDAC a significant DNL error occurs when switching between the 4 thermometer bits and the binary steps in the IDAC, which result at a DNL increase every 16 codes. Besides these artifacts the ADC behaves well and since most of the output range in the imaging application will be dominated by photon shot noise, the ADC performance is sufficient for the purpose. Table 1 summarizes the ADC performance.

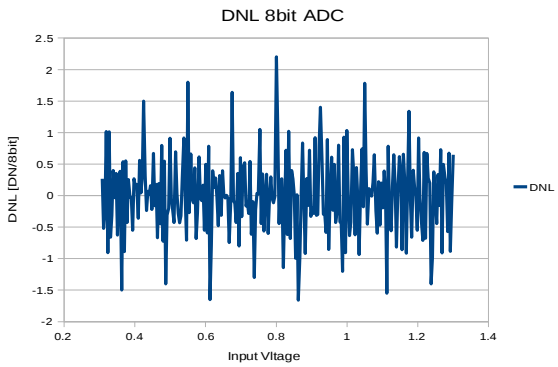

Fig. 4: DNL of the ADC as measured on a separate test chip for characterization purpose.

Area	0.022mm2
Sampling Rate	400kHz
Power consumption	7mW
Bit Resolution	8 bit

Table 1: ADC Performance

3.2 Image sensor over all performance

The complete image sensor was characterized while using a de-serialization to 8bit implemented in an FPGA, which provides recovery of the clock signal embedded in the data stream at every found bit transition. The B&W version of the sensor was characterized using the photon transfer method [10]. Figure 5. shows the obtained results.

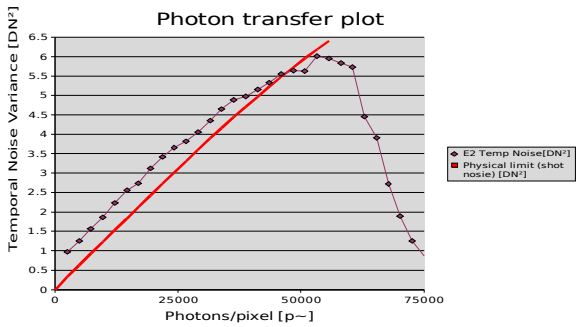

Fig. 5: *Photon Transfer plot, showing the variance of the noise measured with 2m cabling versus the physical shot noise limit.*

A summary of the electrical and optical performance and specification is given in table 2.

Parameter	**Specification**
Supply voltage	1.8V
Total power consumption	26mW
Responsivity B&W	30DN/nJ/cm2
Temporal noise in dark	1.2DN
Bit resolution	8
Frame rate	40Fps
Dynamic range	46.5 dB
Number of pixels	10'000
Color version	RGB Bayer

Table 1: Electrical and performance

Two sample images of the sensor are given in figure 7.

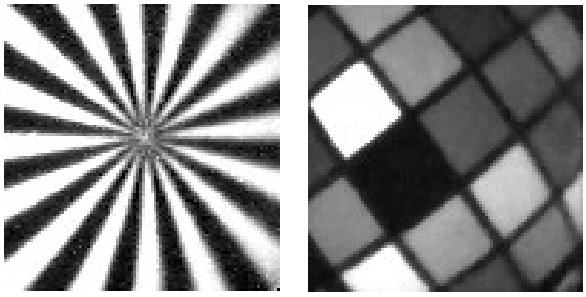

Fig. 7: *Two sample images of the sensor. Left "Siemens star", right McBeth color checker board.*

5 CONCLUSIONS

The presented work shows a image sensor with minimal form factor. To our knowledge the presented work is currently the world's smallest digital image sensor. The availability of such small image sensors opens a complete new filed to medical diagnosis and treatment over minimally invasive procedures. Further improvements on the somewhat disappointing ADC performance of the demonstration sensor have already been undertaken by AWAIBA, which lead currently to comparable sensors exceeding true 9bit performance. The scope of this work to demonstrate feasibility of a SOC imager with only 0.35mm2 chip surface and its usability for endoscopic applications was clearly achieved.

REFERENCES

[1] Kwang-Bo Cho, A. Krymski, E. Fossum, " A 1.5V 550uW 176x144 Autonomous CMOS Active Pixel Image Sensor" IEEE Trans. Electron Devices Vol 50 Jan 2003 pp 96 - 106

[2] Shinya Itoh, Shoji Kawahito and Susumu Terakawa,"A 2.6mW 2fps QVGA CMOS One-Chip Wireless Camera with Digital Image Transmission Function for Capsule Endoscopes", Proc. 2006 IEEE International Symposium on Circuits and Systems B3P-Z, pp.3353-3356, 2006.

[3] Milin Zhang, Bermak, A. Xiaowen Li, Zhihua Wang "A low power CMOS image sensor design for wireless endoscopy capsule" Proc. IEEE Biomedical Circuits and Systems Conference, 2008. BioCAS 2008. pp. 397-400 20-22 Nov. 2008

[4] Dany Scheffer, "Endoscopes use CMOS image sensors" On line: http://www.vision-systems.com/display_article/301875/19/none/none/SPFEA/Endoscopes-use-CMOS-image-sensors

[5] On Line: http://www.ovt.com/uploads/parts/OV6930_PB(1.0)_web.pdf

[6] S. Tanner; S. C. Lauxtermann; M. Waeny; M. Willemin; N. Blanc; J. Grupp; R. Dinger; E. Doering; M. Ansorge; P. Seitz; F. Pellandini "Low-power digital image sensor for still-picture image acquisition" Proc. of SPIE Vol. 4306 pp358-365

[7] M. F. Snoeij, A. Theuwissen, K. Makinwa, J. Huijsing "A CMOS Imager With Column-Level ADC Using Dynamic Column Fixed-pattern Noise Reduction" IEEE JSSC Vol. 41, No 12 DEC 2006 pp 3007-3015

[8] M. Scott, B. Boser, K. Pister " An Ultralow-Energy ADC for Smart Dust" IEEE JSSC Vol. 38. No 7 July 2003 pp 1123-1129

[9] K. Tanaka, Y. Kuramochi, T. Kurashina, K. Okada, A. Matsuzuwa. " A 0.026mm2 Capacitance-to-Digital Converter for Biotelemetry Applications Using a Charge Redistribution Technique" Proc. EEE ASSCC 2007, 9-1 pp-244-247.

[10] Janesick, James R., CCD characterization using the photon transfer technique, Proc. SPIE Vol. 570, Solid State Imaging Arrays, K. Prettyjohns and E. Derenlak, Eds., pp. 7-19 (1985)