

Enhancement of Wide Dynamic Range CCD with 862MHz Data Rate

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ABSTRACT

A 52-M pixel, 71mm x 54mm, full-frame CCD imager with $8.6 \times 8.6 \text{ } \mu\text{m}^2$ pixel size has been developed for use in high speed scanning applications. On-going interest for ultra-high resolution, high speed imagers for electronic imaging OEM customers in various scientific markets including spectroscopy and digital photography has lead to the development of the STA2500A. Innovative design techniques were utilized in the production of this device. 32 outputs running at 20 Mhz yield a 10Hz frame rate with low RMS noise, 68dB dynamic range, and high MTF. This paper will provide detailed information on design trades developed for high-speed imagers leading to the design and performance capabilities of the STA2500A, as well as a description of the electronics required for its use.

Key Words: Charge Coupled Device (CCD), Charge Transfer Efficiency (CTE), RMS Noise, Quantum Efficiency (QE)

1. INTRODUCTION

As traditional imaging applications move into the digital realm, the device specifications become extremely critical. The STA2500A was designed to provide industry with high resolution, high dynamic range, high speed, low noise devices that can be implemented in industrial regions ranging from medical imaging to digital film scanning. For example image array size, noise, and dark current are critical in spectroscopy, biological imaging, and x-ray tomography. On the other end of the spectrum are digital photography and digital film scanning which require high resolution and high speeds, while maintaining low noise and reduced image defects. Currently the digital film scanning market is controlled by linear TDI (time-delay integration) CCD's or CMOS devices that lack dynamic range and physical size. The STA2500A design, fabrication, and readout electronics were manufactured to fit the needs of the latter high frame rate OEM customers.

2. STA2500A DEVICE DESCRIPTION

The STA2500A is an 8320 x 6320 image element solid state Charge Coupled Device (CCD) Full Frame sensor. This device is depicted schematically in Figure 1, exhibiting split frame transfer configuration. The vertical clocks are configured such that there are eight individual sections that reduce the overall capacitance per clock driver. This improves the vertical charge transfer efficiency (CTE), as well as reduces the risk of image smear at high frame rates. This CCD is intended for use in high-resolution scientific, space based, industrial, and commercial electro-optical systems. The STA2500A is organized in two halves each containing an array of 8320 horizontal by 3160 vertical photosites. There are 32 outputs, 16 outputs per serial register, allowing for increased frame-rates. For dark reference, each readout line is preceded by 8 dark pixels. This imager is available in a full frame configuration or a split frame transfer configuration with shield metallization covering half of the imager. The split frame transfer architecture allows higher frame rate operation through four readout quadrants, whereas the single-sided approach allows readout through two readout quadrants. The STA2500A can be offered as a backside illuminated version for increased sensitivity and UV response in the same package configuration, or with optional Vertical Anti-blooming via a vertical overflow drain structure (VOD).

Figure 2 represents an individual output imaging subset of the STA2500A. These individually addressable output sections reduce the number of horizontal transfers, thus improving the horizontal CTE. The pixel size is $8.6 \times 8.6 \text{ } \mu\text{m}$ in the imaging array; however the horizontal register is designed to store two times the vertical full well for binning. The output is a dual stage FET that is operable at readout rates up to 40MHz. This device was fabricated using a three-phase, triple poly, triple metal process. The STA2500A has the capability of capturing data at a rate greater than 20 frames per second.

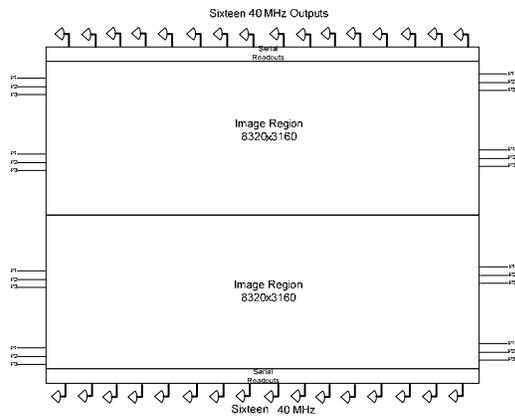


Figure 1. Schematic of STA2500A Imager.

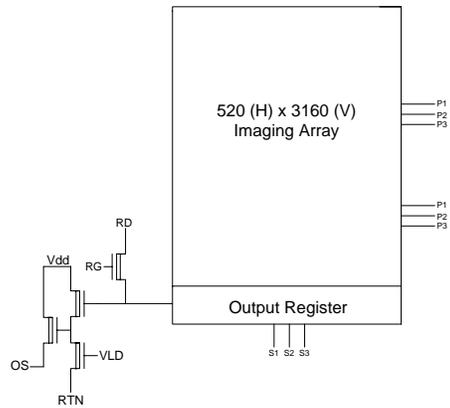


Figure 2. Schematic of the STA2500A Imager Subcell.

These devices are fabricated using a mixed mask process (combining 1x and 5x stepper masks) that allows for internal strapping of the vertical gates. This decreases the RC time constant by reducing the series resistance of the polysilicon gate, thus enabling an increased vertical clock rate. To further improve the readout speed and performance, the drive electronics and output buffer stages are placed on a header board and incorporated in the package. This is shown in Figure 3. The sensor is packaged on an aluminum substrate with low thermal resistance allowing for better temperature control. The substrate material is subject to change depending on the temperature requirement. For cold applications we typically use Invar36 or Molybdenum.

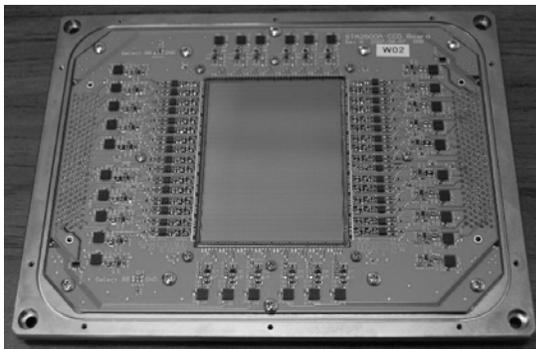


Figure 3. STA2500A Imager with Drive Electronics

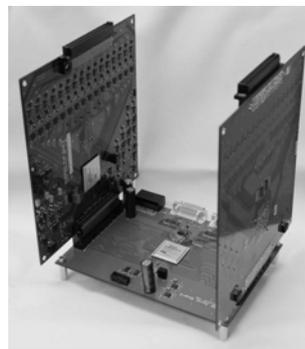


Figure 4. STA2500A Readout Electronics

3. STA2500A ELECTRONICS DESCRIPTION

The electronics for running the STA2500 imager supply the necessary DC biases and clock signals for operating the CCD, as well as digitize the output signals. The system consists of a CCD board, two AD boards, and a backplane as shown in Figure 4.

The DC biases are derived from digital potentiometers, and buffered using filtered op-amp circuits. This yields an accuracy of 0.01 Volts. The clocks are AC-coupled to the CCD, using Supertex MD1210 drivers for the serial and reset signals and Intersil EL7156 drivers for the image area clocks. The CCD is mounted to an aluminum block, and the PCB wrapped around the CCD is also mounted to the aluminum block. Good thermal contact between the PCB and block is maintained using a thermal interface pad. The aluminum block can then be cooled to remove the heat generated by the high speed clock drivers the power dissipation is on the order of 20W at 20 MHz, therefore active cool is required. For room temperature operation this can be accomplished with water cooled manifold or a heat sink with an attached fan. For colder applications thermal electric coolers (TEC) are utilized to remove the heat.

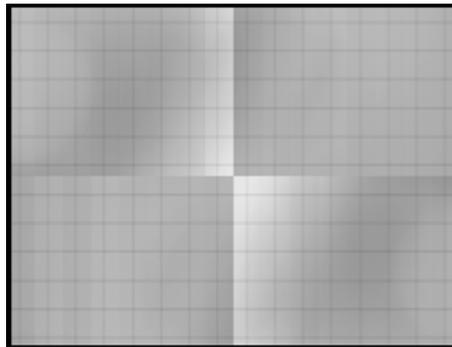
The clock drivers and output buffers are mounted as closely as possible to the CCD to minimize transmission line effects and crosstalk at these high clock rates. Each clock driver circuit has a logic-level input supplied from timing cores on the other boards, a high current clock magnitude voltage (typically 8 to 12V), and a low current DC clock level. The DC clock level is set to the "resting" state for that clock (which may be high or low depending on the clock), and coupled to the CCD clock line with a diode and resistor in parallel to force the CCD clocks to the desired levels. This scheme was necessary because of the limited voltage range of the clock driver ICs. In particular, the low level of the image area clocks (typically -9V) is out of specification for the chosen drivers.

The CCD outputs have a simple resistive load. The video signal is then AC-coupled into low-noise, fast-settling op-amps directly adjacent to the CCD (AD8045s). The buffered video signals are routed to an attached AD board. Coarse gain selection is done using a high-bandwidth multiplexer (ADG1204) to accommodate the increased signal levels when binning. The signal is buffered and filtered, and then digitized by an array of AD9970 analog front ends (14-bit, 65 MHz max, 2.0 DN noise). In addition to DC-restore, correlated double sampling and digitization, the AD9970 also generates the timing for the serial and reset clocks.

Each AD board has 16 AD9970s, for sampling 16 CCD outputs. The AD9970 uses high speed LVDS to output the digitized samples, with one clock pair and two data pairs. For a 20 MHz pixel clock, the AD9970 LVDS clock is 80 MHz DDR. All AD9970 LVDS pairs go to a Xilinx Virtex 4 FPGA. The FPGA is programmed with a variety of functionality. It includes a timing core that generates frame and line timing, and can be modified on the fly. The FPGA also contains a Picoblaze processor which communicates over a simple serial interface, and is responsible for configuring the AD9970s, DC biases, and all other secondary board ICs such as temperature sensors.

The system to run a full STA2500 contains two 16-channel AD boards, which plug into a backplane board. The AD FPGA relays all samples to the backplane over a 160 MHz DDR 14-bit bus (at a 20 MHz pixel clock) to an FPGA on the backplane. The backplane FPGA is also a Virtex 4, which selects data from 8 of the 32 CCD outputs and transmits it over a full CameraLink interface to a host computer for display. A full 64-bit CameraLink interface at an 80 MHz clock rate can sustain a data transfer rate of 640 megabytes per second, which is enough for 8 14-bit taps at a 40MHz pixel clock. Capturing all 32 outputs at a 40MHz pixel clock implies a 2.56 gigabyte per second data rate, which means using either four full CameraLink interfaces or a custom data acquisition platform.

4. STA2500A PERFORMANCE



STA2500A Full Resolution Image (Uncorrected)

4.1 Full Well

The full well is the amount of signal the CCD is able to store in a single pixel potential well without spilling charge into adjacent wells. This sensor had average full well signal levels greater than 750mV, which is equivalent to approximately 75ke-. The full well measurements were taken using photon transfer curve method. The Photon Transfer Curve (PTC) is a plot of noise versus signal for a digital sensor.³ Figure 5 is the measured PTC including the pixel full well capacity. These results are also given in Table 1.

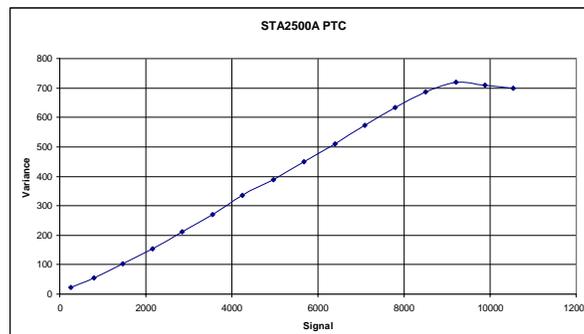


Figure 5. Photon Transfer Curve

4.2 Signal to Noise Ratio

The signal to noise ratio, or dynamic range, is the ratio of the maximum usable signal to the RMS noise of zero signal. This is found by taking the ratio of the full well to the RMS noise level found in the dark pixels of the imager. Dark current noise contribution will be negligible due to readout rates. This is shown in Table 1 along with the related noise measurements.

4.3 Responsivity

One of the most important aspects to a high quality imager is the responsivity or quantum efficiency. This is the ability of the imager to collect photons created at varying spectral bands. During the early development of this project STA studied the effect of polysilicon thickness on the device quantum efficiency. Research proved that by decreasing the thickness of the polysilicon gates the broadband quantum efficiency is improved. A thick poly-gate structure typically peaks near 650 nanometers and the photons begin to be absorbed by the gate at wavelengths beyond this point. By decreasing the thickness of this gate structure the absorption characteristic is pushed into the NIR, improving the overall quantum efficiency of the device. Figure 6 charts the results of this experiment. The responsivity of the STA2500A was measured in diode mode, where the reset drain current is measured over varying wavelength and compared to a calibrated photodiode. Using a MS257 Monochromometer with a 10um slit, and a Quartz-Tungsten-Halogen (QTH) lamp the devices are measured at every 50nm between 400nm and 1000nm. In Figure 6, the greater average responsivity represents that measured for the STA2500A.

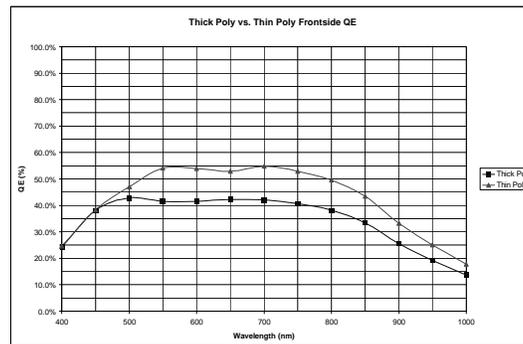


Figure 6. Thick Poly vs. Thin Poly Quantum Efficiency

4.4 Photo Response Non-Uniformity

The CCD photo-response non-uniformity (PRNU) is a measurement of fixed pattern noise. If a device is illuminated uniformly, there will be an average charge level collected by the pixels and a variance in charge about this mean. This is related to a variation in pixel sensitivity. The STA2500A CCD was measured with a uniform illumination image taken at 530nm. The results are found in Table 1.

4.5 Image Lag (Charge Transfer Efficiency)

Image lag is a measurement of photosite to CCD shift register transfer loss and horizontal register to sense node transfer loss, due to imperfect charge transfer from gate-to-gate within the CCD. For example, when a pixel is illuminated, and the resultant photocharge is transferred to the horizontal CCD less than 100% of the charge is transferred; the remaining charge appears in subsequent lines. This degrades MTF. This effect is especially apparent when several dark/black lines immediately precede or follow several illuminated lines. This can also be related to smear, however will not improve with the reduction of vertical clock speeds.

These effects were measured using uniform illumination and a method called Extended Pixel Edge Response (EPER). The illuminated light level was adjusted between about 1%, 50%, and 75% signal level of saturation. An image, containing vertical and horizontal extended pixels, was taken at each illumination level.

$$CTE_x = 1 - \frac{S_b(e^-)}{S_{LC}(e^-)N_f} \quad (1)$$

The charge transfer efficiency (CTE) was measured using Equation 1. Where CTE_x is the charge transfer efficiency measured by EPER, S_D (e-) is the extended pixel signal, and S_D is the average deferred charge after N_p pixel transfers.¹ The STA2500A has a measured horizontal CTE of 0.999998, and a vertical CTE of 0.99998.

4.6 Linearity

The CCD light-to-voltage chain is not perfectly linear, and some degree of nonlinearity is expected. In particular the output charge integration node and output amplifier are the primary source of nonlinearity. The linearity of the STA2500A was calculated using the camera gain constant as a function of signal¹. We utilized a pseudo-TDI image method to collect the data necessary to plot the linearity curve.² The results are given in Table 1.

5. Conclusions

The STA2500A 52-Mega Pixel imager is capable of providing high quality imaging for multiple markets. The focus behind this design was to meet current and future industrial needs, including high frame-rates, high resolution, and high quality imager cosmetics. Future device improvements include increased vertical clock rates, increased sensitivity for low light imaging, and anti-blooming for over exposure. This paper exemplifies STA's efforts to revolutionize the OEM electronic imaging market, thus paving the road for the future of CCD imaging.

STA2500A Performance Specifications	
Pixel saturation voltage (VSAT):	750 mV
Readout saturation charge in binning mode (RSAT):	2250 mV
Non-binned Dynamic range (DR) @ 20MHz:	68.5 dB
Non-binned Dynamic range (DR) @ 40MHz:	57 dB
2 x 2 Binned Dynamic range (DR):	80 dB
Readout noise @ 20 MHz 3-stage Source Follower (RN):	27 electrons
Readout noise @ 40 MHz 3-stage Source follower (RN):	38 electrons
Responsivity (R):	4 V/(μ J/cm ²)
Output mismatch:	<2%
Pixel response non-uniformity (PRNU):	<1% (standard deviation)
Image zone dark signal (DS):	20 pA/cm ²
Horizontal charge transfer efficiency per CCD stage (HCTE):	99.9995%
Vertical charge transfer efficiency per CCD stage (VCTE):	99.9980%
Operating temperature	25°C, typical voltage.

Table 1. STA2500A Performance Specifications

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