An analog counter architecture for pixel-level ADC

Arnaud Peizerat, Michael Tchagaspanian, Christophe Mandier, Bertrand Dupond

CEA/LETI - MINATEC
17 avenue des Martyrs, 38054 Grenoble, France
arnaud.peizerat@cea.fr

***Abstract*—Pixel-level ADC is often used for applications that does not require small pixel (IR and X-ray imaging). In that case, the pixel changes a charge packet into a pulse that feeds the input of its own counter. This paper presents the advantages of an analog counter against a digital binary one.**

We use a 0.18µm CMOS process to study a new compact analog counter architecture inspired by neural network literature [3] or medical imaging literature [4]. Simulation and measurement results show that area and noise pollution benefit from this analog counter.

I. INTRODUCTION

The point of a pixel-level A/D conversion is first, power reduction, through a lower conversion frequency, and second, noise reduction, because the noise associated to analog multiplexing is avoided [1]. The main constraint is the limited pixel area which explains that the concerned applications are mainly IR and X-ray detections (large pixels) rather than visible imagers (small pixels).

We developed two architectures of digital pixel [2]. The common principle which consists in counting charge packets coming from the detector is also called charge-balancing technique [5]. As illustrated in Fig. 1, the photocurrent, created by the illumination, discharges C_{int} until V_{int} crosses V_{ref}, then the comparator commands the injection of Q_0 ($=C_{int}.\Delta V$) at the integration node and the counter is incremented by one. At the end of the integration time, the counter contains the number N. Since the LSB value of the A/D conversion is Q_0, $N.Q_0$ has been detected. The only difference between the two techniques is the way Q_0 is generated. In the "voltage reset" case, $Q_0=C_{int}.\Delta V$ and consequently the LSB is highly dependent on V_{ref}. This technique is thus very sensitive to the performance of the comparator but allows an efficient layout. In the "charge reset" case, Q_0 is generated by a charge injector, thus it relaxes constraints on the comparator and on C_{INT} precision, providing the charge injector has good performance.

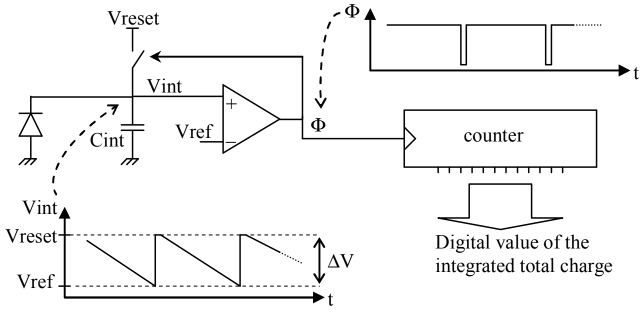


Figure 1. principle of the pixel-level ADC techniques in [2], assuming the phocurrent is constant

Both techniques need a binary counter per pixel. For the sake of simplicity, this counter is designed as an asynchronous binary counter, occupying 75% of the readout electronic surface of the pixel. This paper presents how we use an analog counter to mainly reduce the required counter area.

Section II describes the design of the analog counter and how it modifies the imager architecture. Section III shows the experimental results we obtain on a test-chip with a 0.18µm CMOS process. Finally we give some details on the future work we plan to do.

II. ANALOG COUNTER DESIGN

The idea consists in transferring small charge packets onto a capacitor each time the counter is fed with a falling edge of the clock. So the resulting output curve is a step curve as shown in Figure 2. One can note that the signal V_{carry} is also needed if several analog counters are cascaded. At the end of the integration time, the output of the pixel is the analog output value(s) of the counter(s).

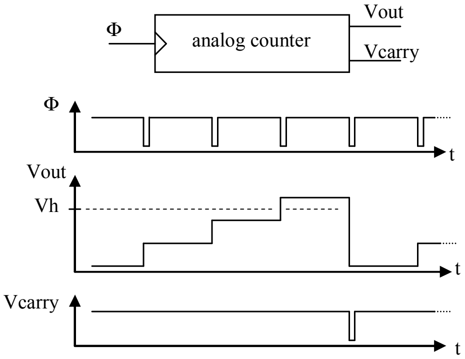


Figure 2. targeted input and output signals for a 4-level analog counter

This value is then read-out and digitalized by a column-level analog-to-digital converter. Therefore the key point is to split complexity between the pixel and the bottom of the column, i.e. between the analog counter of the pixel and the column-level ADC.

An example of such an imager architecture is given in Figure 3. The pixel contains five cascaded analog counters, the output values of each counter consisting in only 8 analog values. Consequently, while the resolution of the column-level ADC is of 3 bits only, the total resolution is of 15 bits.

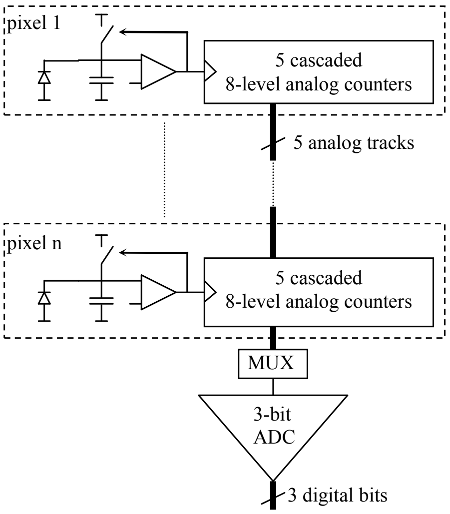


Figure 3. architecture of one column for an imager when using 5 cascaded 8-level analog counters

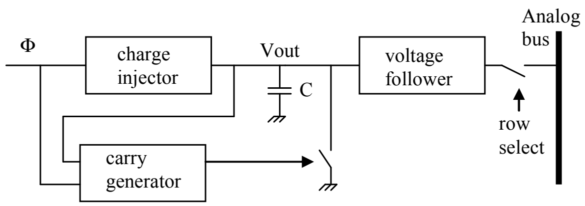


Figure 4. block scheme of the analog counter

The analog counter can be subdivided into three blocks as illustrated in Figure 4. The charge injector transfers a certain amount of charge onto the capacitor C for each pulse of Φ. This function is obtained thanks to one of the two schemes ([2], [3]) on Figure 5.

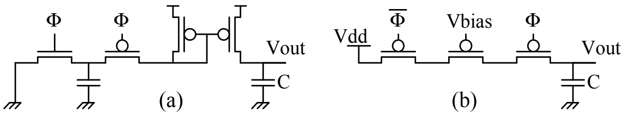
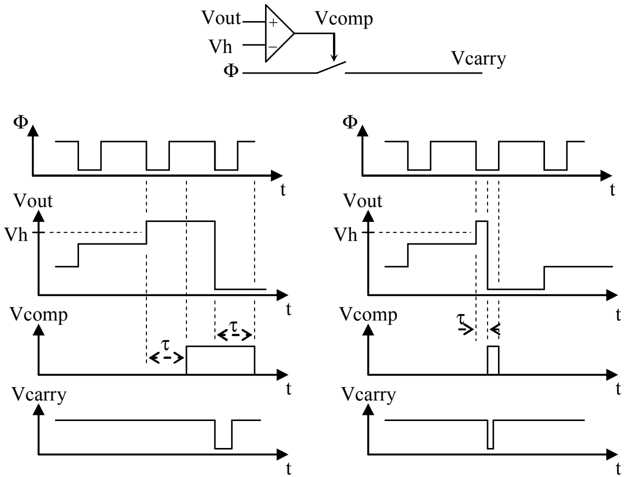


Figure 5. charge injectors (a) in [3] and (b) in [2]

The linearity of the charge injector in [2] is better than that of the one in [3]. But this assumption is only true if a linear capacitor C is available. In our case, the use of MOS capacitance is essential as the main goal of the design is to reduce the layout area. That is the reason why the charge injector of [2] associated with a PMOS capacitance is the solution that gives the best trade-off between linearity and compacity.

The second block generates the carry of the counter. It consists in a switch and a comparator. The main feature of the comparator is its delay τ that has to be above the duration of the pulse of Φ, as shown in Figure 6. The biasing of this comparator is then very low, i.e. below 100 nA.

The third block allows the readout of the analog value on the capacitor C. As linearity is of importance, the source follower scheme cannot be used. An OTA composed of a PMOS differential pair is thus preferred. The layout of this follower can be small as well, as the current mirror and the current source can be implemented at the column-level. The snapshot function can be carried out thanks to the use of two OTAs, two C capacitances and two switches as illustrated in Figure 7.



(a) (b)

Figure 6. timing diagrams when the comparator delay τ is (a) above and (b) below the pulse duration of Φ.

Such an analog counter shows a 50% reduction in the size of its layout in comparison to an asynchronous binary counter composed of static DFFs.

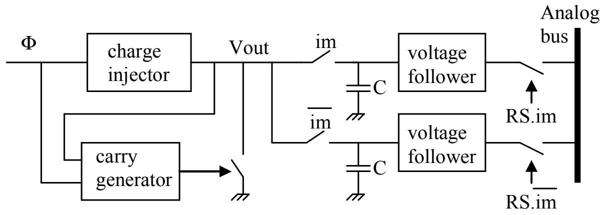


Figure 7. block scheme of the analog counter with the snapshot feature

The number of analog levels is limited by technological fluctuations and noise considerations. Simulation shows that a sixteen-level counter does not have a sufficient noise margin between two consecutive levels. Figure 8 illustrates a good result of an eight-level counter for a Monte-Carlo analysis. One can note that the main contributor is the charge injector as the step of the curve goes thicker regarding the analog level.

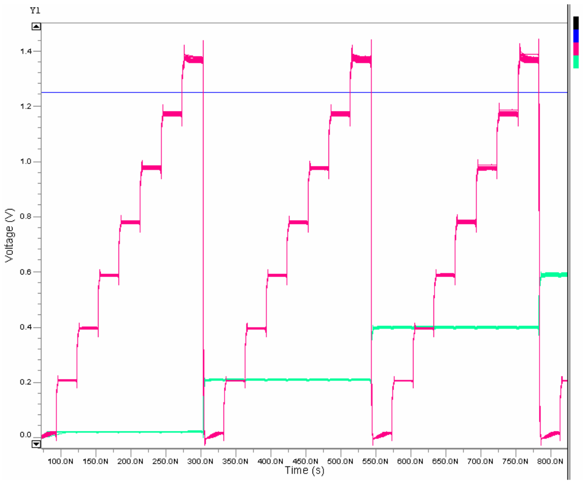


Figure 8. simulated pixel outputs of the first and second analog counters for a 100 run Monte-Carlo analysis

III. EXPERIMENTAL RESULTS

A test-circuit was fabricated in a 0.18 µm process with 1.8V and 3.3V power supply voltages (Figure 9). As the objective is to fully characterize the new analog counter rather than to carry out an image sensor, this test chip only contains 2 columns of 16 pixels and each pixel is solely composed of the analog counter. Pixels' inputs are thus fed with a tunable pulse signal that is implemented on-chip so that a small pulse width can be achieved. An additional pixel separated from the others is also used to probe some of the internal signals. Some measurement results are given in Figure 10.

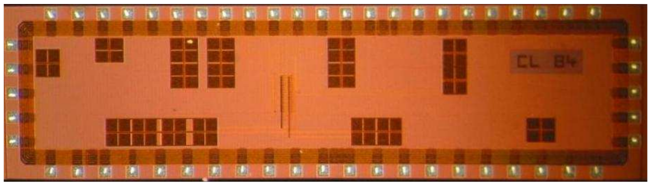


Figure 9. photograph of the test-chip

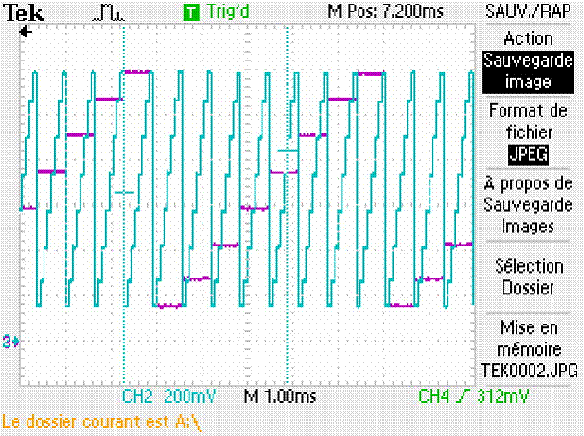


Figure 10. measured pixel outputs of the first and second analog counters on the test-chip

The minimum power consumption is estimated at 30nA per counter. When using 5 cascaded 8-level analog counters per pixel in order to achieve 15 bits per pixel, it gives 150nA per pixel.

IV. CONCLUSION

An analog counter for pixel-level ADC has been described. Design considerations and measurement results have been given and show the functionality of such a counter with a 50% reduction in the layout.

The next step will consist in the design of a whole imager. A reduction in the pixel pitch from 25µm to 17µm is targeted for infra-red applications.

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