

## 2009 International Image Sensor Workshop

### CMOS Active Pixel Detectors For Radiography

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#### Abstract

Use of CMOS active pixel image sensor technology in radiological applications is growing due to the low noise, wide dynamic range, and competitive costs that can be achieved. As tiled CMOS focal plane technology matures and begins to compete with large area TFT- based X-ray detector panels, CMOS radiographic sensor technologies are tailored to optimize performance. Not surprisingly, the usual suspects of read noise, full well capacity, responsivity, resolution, dark current, and frame rate dominate the list of features most requested for improvement. Added to the list is the radiographic performance measurement of DQE that characterizes the CMOS sensor and X-ray conversion components in the multi-layered detector. Tolerance to ionizing radiation is a parameter that ultimately relates to cost and may be part of the CMOS technology or the detector construction.

Design of large pitch 3T CMOS APS pixels, as used in radiological detectors, is simplistic compared to that of advanced visible detectors. However, the variety of X-ray imaging applications, from pipe weld inspection to mammography, and from dental CT to protein crystallography, create a demand for the CMOS sensor technology to accommodate the broadest range of performance in a single detector design. To make this accommodation requires pixel engineering to optimize conversion efficiency while minimizing dark current and kTC noise, as well as maintaining yield for very large die areas. The sensor architecture must allow for close tiling and support higher frame rates, and the markets demand that large area tiled detectors provide adequate resolution, reduce dosing, and provide radiation damage protection.

We will discuss the engineering of CMOS APS pixels and features of sensor architecture specifically adapted for radiographic panel fabrication. Included will be results from experiments in sensitivity gain through photodiode capacitance variation. Full panel X-ray performance testing of tiled CMOS detectors will be discussed and include data for cameras with 20cm x 20cm active area. Data from new applications, including Laue X-ray diffraction studies of protein crystals, will also be presented.

Figures 1 through 4 illustrate the sensor architecture for a three side tileable CMOS APS array, pixel engineering for voltage response increase, sample images of tiled image sensor performance, and mean variance plots several pixel capacitance variations.

Fig. 1A

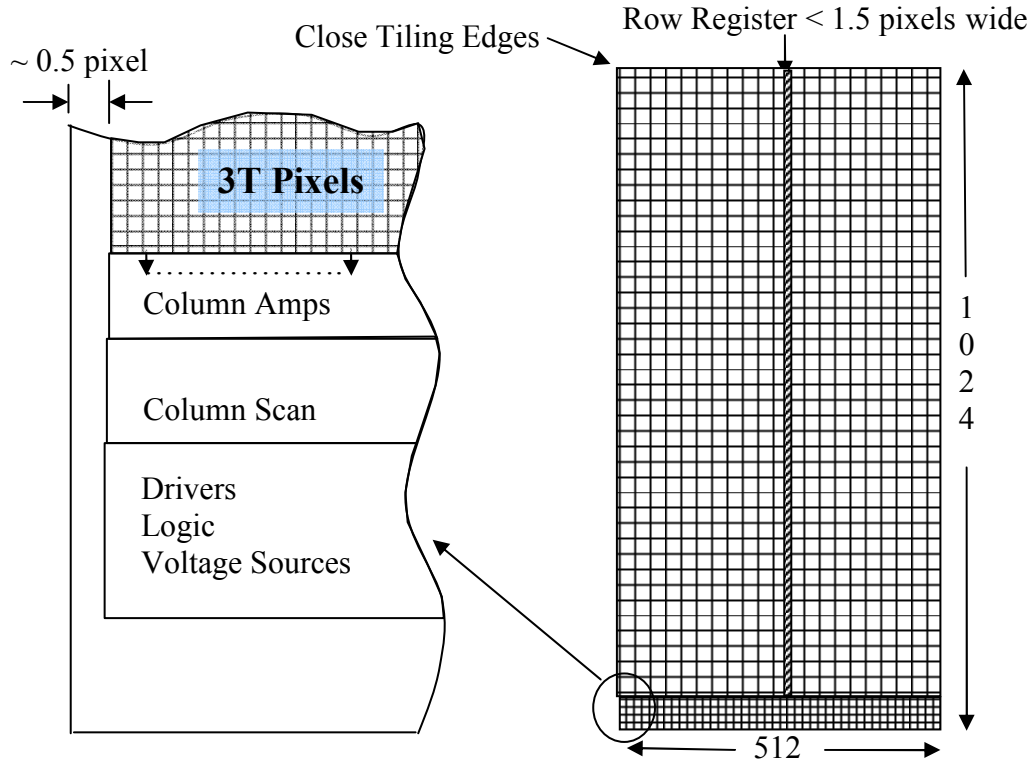
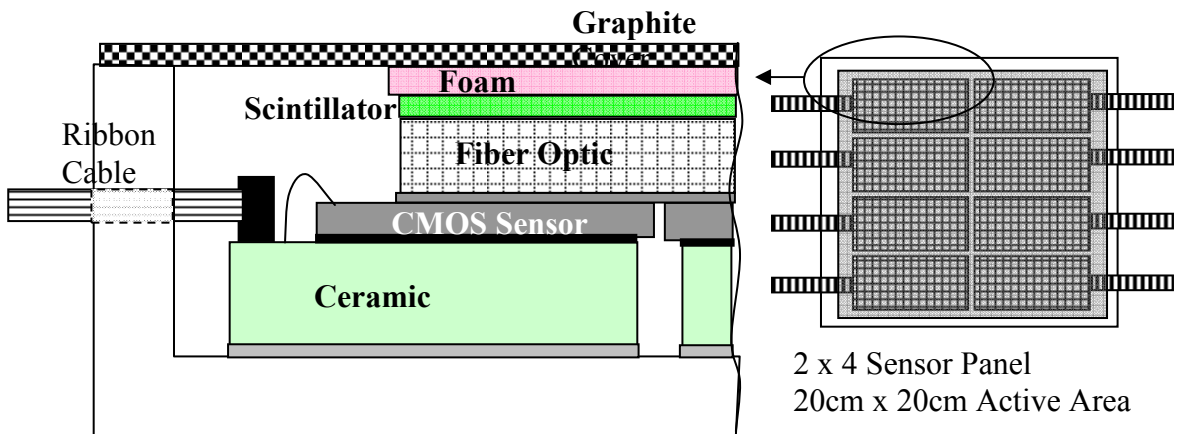


Fig. 1B



Figures 1A, 1B Three side tileable CMOS sensor, Tiled detector cross section

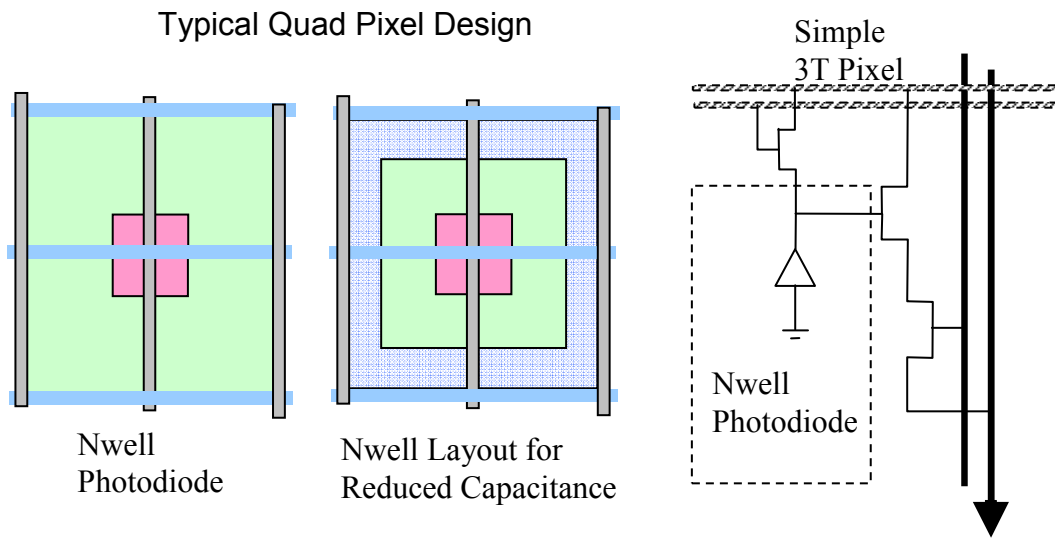


Figure 2 Example of Voltage Response Engineering in the Large Pixel

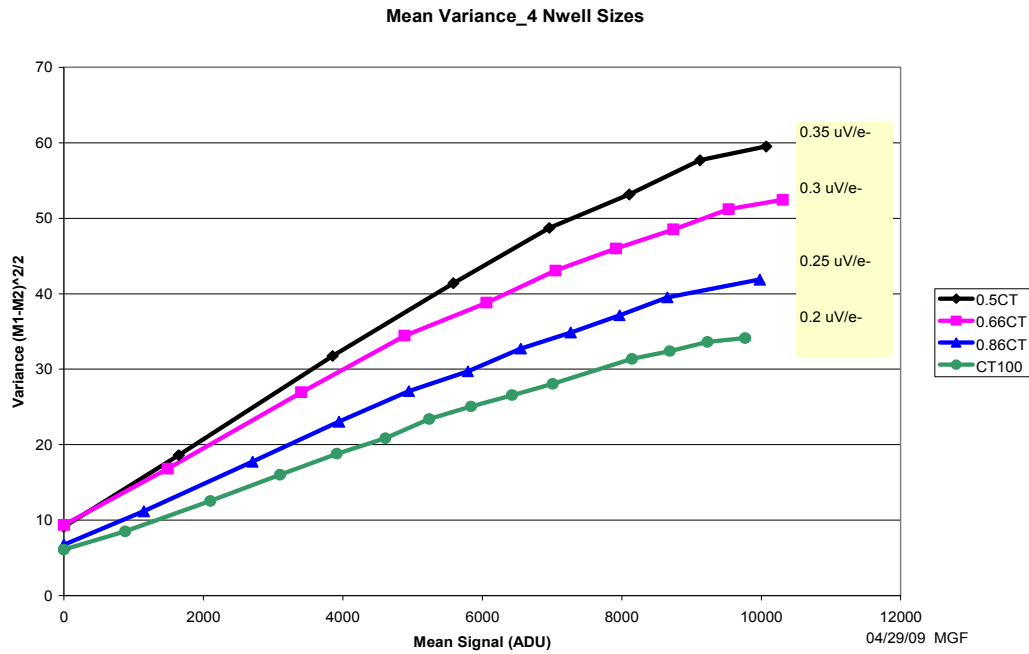


Figure 3 Mean Variance for several pixel Nwell layouts

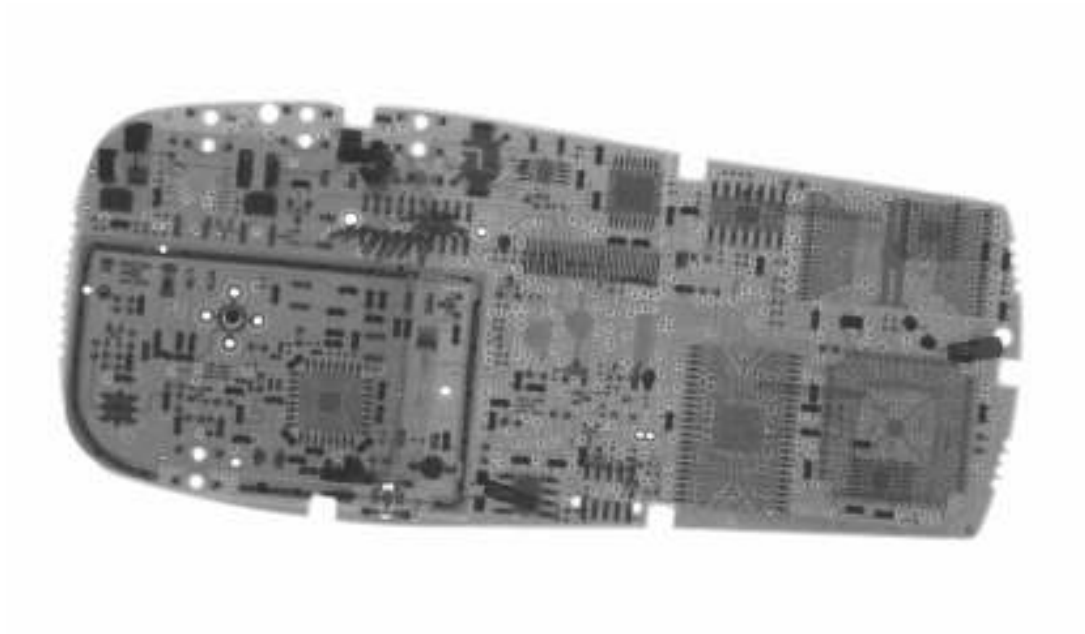


Figure 4 X-ray Image of cell phone pcb – across three tiled sensors