

A 4k@15,000 LPs High-Accuracy CMOS Linear Sensor Chip with Programmable Gain and Offset and Embedded Digital Correction

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Introduction

Machine Vision (MV) applications require high quality images and hence dedicated CMOS technologies (CIS) and optimized pixels such as for instance those based on pin photodiodes. High-performance CMOS MV sensors with image moving capture, exposure control, anti-blooming, high-speed readout, etc have been devised elsewhere using these CIS technologies [1]. However, most of them require off-chip digital processors for correction of the raw sensor data, which has an impact on power, reliability and compactness.

This paper reports a CMOS tri-linear image sensor with and *on-chip embedded digital processor* for MV. This *single chip smart sensor* is conceived to reach performance levels similar to those of multi-chip CCD digital camera systems [2]. Table 1 summarizes data of available linear sensors, including a CCD one to the purpose of performance comparison. The last column corresponds to the device reported in this paper, called AFLS4k. The AFLS4k performs similar to the CCD one and has better accuracy specs than its CMOS counterparts.

Table 1 – Comparative Performance Data for Line-scan image sensors

	DRAGSTER 4k	spL4096	DLIS-4k	IT-P1-4k	AFLS 4k
Technology	CMOS	CMOS	CMOS	CCD	CMOS
Producer	Awaiba	BASLER	Panavision	DALSA	ANAFOCUS
Pixel size [μm]	7 x 7	10 x 10	10 x 10	10 x 10	7 x 7
Well capacity [e⁻]	45k	N/D	N/D	150k	55k
Pixel count	1 x 4k	2 x 4k	2 x 4k	1 x 4k	3 x 4k
Dark current impact (mV/sec)	5	N/D	2.8	1.5	5
Quantum efficiency at 550nm [%]	50	50	N/D	90	60
PRNU_{RMS} [% output range]	3	N/D	N/D	6	0.2
DSNU_{RMS} [% output range]	0.5	N/D	N/D	~0	0.01
Saturation exposure (SEE) [nJ/cm²]	N/D	N/D	N/D	65	47.6
Minimum exposure (NEE) [pJ/cm²]	10	N/D	N/D	20	13
Line rate [lines/second]	40,000	19,300	8,000	23,700	15,000
A/D conversion accuracy [bits]	10	12-10-8	10	N/A	12
Dynamic range	2200:1	N/D	500:1	3200:1	3500:1
Power consumption [W]	0.8	N/D	N/D	>1	0.5

N/D – No public data available or pending to measure

Matching CCD performance was one of the AFLS4k design targets. Other targets were *re-configurability* and *stand-alone operation* without off-chip digital correction/calibration required. Regarding re-configurability, and in addition to *binning*, *windowing* and *sub-sampling* functions, AFLS4k features *digital control* of both the *gain* (-6dB to +21dB) and the *offset* (±500mV) of the readout channel. All configuration possibilities are made accessible to the user through a simple 4-wire SPI port.

Sensor architecture

Figure 1 shows a block diagram of the sensor including the digital image processor block and the digital camera controller section.

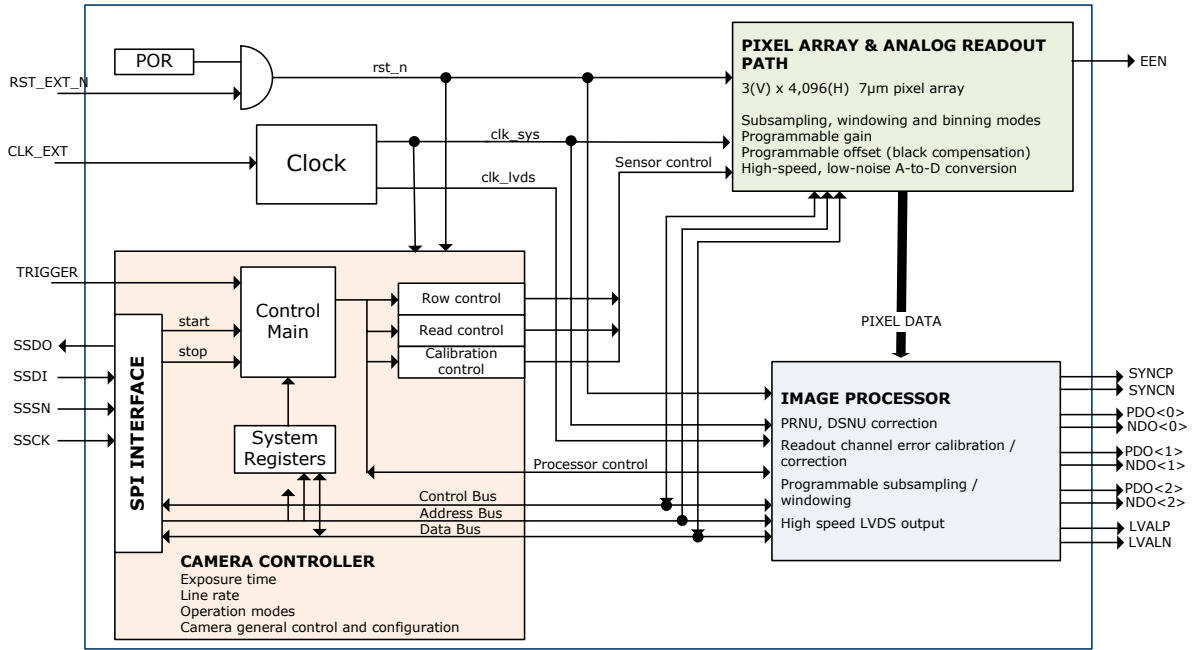


Figure 1. Functional block diagram of the AFLS4k sensor

A 12-bit high-speed low-noise A/D converter is used to digitize the analog data. The resulting digitized pixel data is passed to the embedded image processor. Here pixel-to-pixel gain and offset coefficients are applied to the digitized pixel values to correct DSNU, PRNU, and shading. High-speed digital pixel data are communicated to the outside through three high-speed LVDS drivers. The CC section controls the sensor core to maintain the desired exposure and to support the sensor read-out modes.

Pixel and read-out channel

Figure 2 shows the pixel schematic consisting of four transistors and one pinned photodiode. It also shows the control signals applied to operate the PPD active pixels. The process starts with a full-reset of the PPD raising the reset (R_{st}) and the transfer gate (T_{rf}) signals simultaneously. In this situation any charge in the pinned photo-diode and in the FD node is drained via the transfer and the reset transistors. Then the transfer signal (TG) is lowered, the exposure starting at this point. Shortly afterwards the reset signal is lowered as well. A sufficient exposure time is allowed. Afterwards, the reset signal is raised again for a time Rst_on , and then lowered. This resets the FD node and such reset level (N) is read-out.

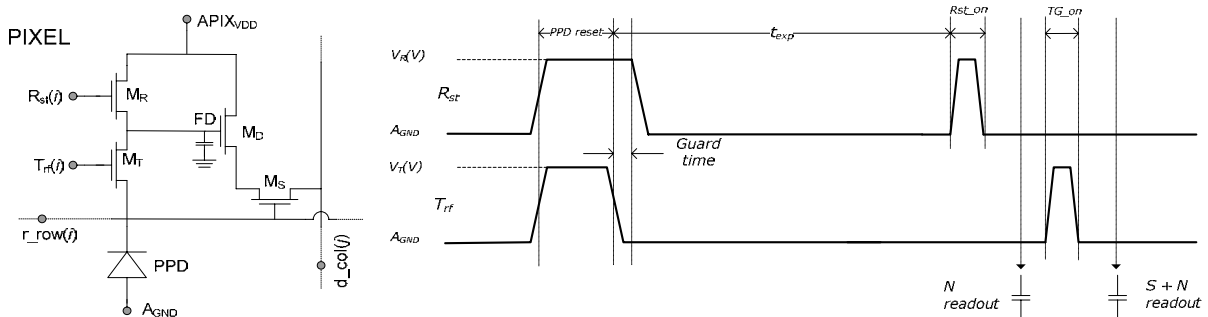


Figure 2. Pixel and control signals

The voltage level at this point is taken as reference. Then, the transfer signal is raised for a time TG_on and then lowered. This results in transferring the charge from the PPD to the FD node. The resulting voltage increment in the FD node is taken as the pixel signal. Such voltage level (S+N) is read-out from the pixel. Reset noise cancellation $\{(S+N) - (N)\}$, is accomplished with the Correlated Double Sampling (CDS) process in the read-out path. The acquisition of the next pixel line will repeat the complete process.

Figure 3 shows a conceptual block diagram of the readout channel with the entry points for offset and gain control.

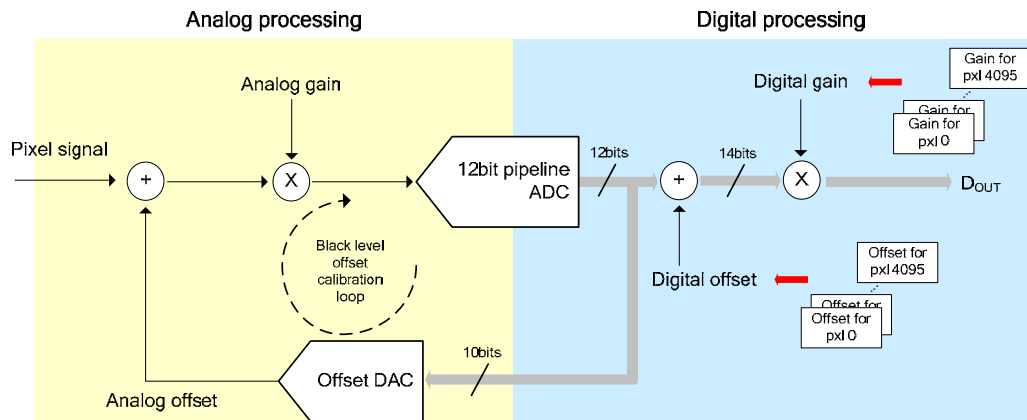


Figure 3. Block diagram of the read-out channel

A mixed-signal programming strategy (one piece of the programming range in analog domain, and other part in digital domain) is employed for optimum design trade-offs. Overall programmability enables optimum exploitation of the ADC input range and gives users the possibility of performing white balance in camera systems 3 sensors to handle color images. The readout channel itself employs an innovative *tree-architecture* with *dynamic element matching selection* to meet the speed requirements with a single 12bit@70MHz data converter per the whole sensor. With reference to Figure 4, the pixel output voltage at the column-data line (the source follower output node) is double-sampled by the DS circuit. The result of the double sampling (and subtraction of the two samples) is the elimination of the Fixed Pattern Noise (FPN) introduced by the pixel-column readout buffers and the reset (thermal) noise of the pixel associated to the sampling of the reset level at the floating diffusion node.

The output of the DSH amplifier consists of a differential signal equal to the signal level of each pixel. The analogue offset circuit subtracts the offset level corresponding to the dark current level from such signal. This analogue offset can be programmed by the user with a 9-bits control word. It sweeps in the analogue range of $\pm 500\text{mV}$ at the input of the ADC. The resolution associated to this offset is 5mV.

The offset signal is generated with a DAC. The maximum and minimum DAC reference levels are programmable through dedicated configuration registers.

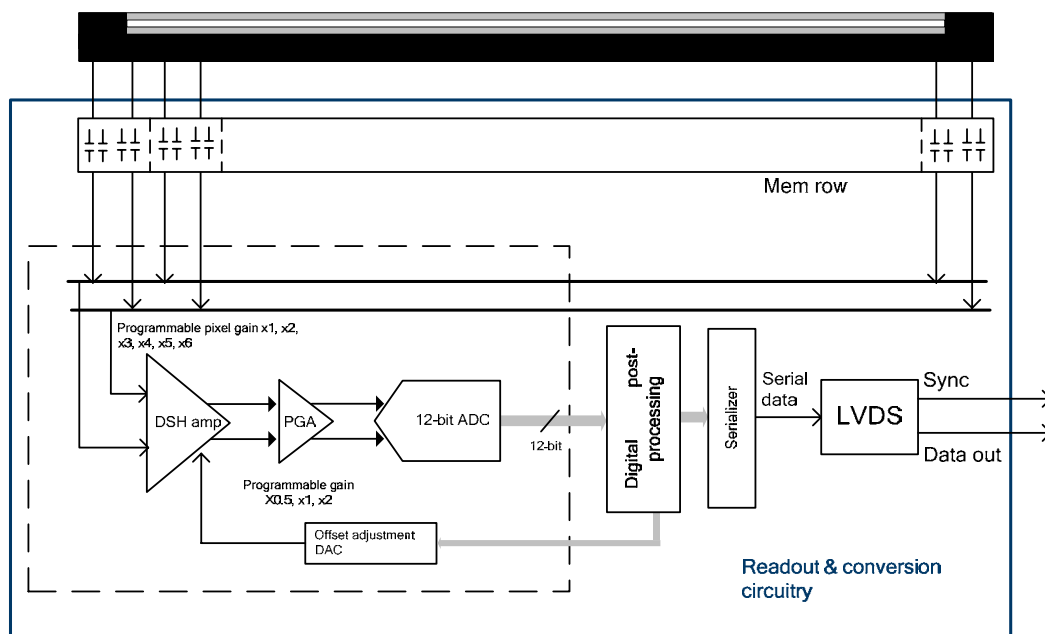


Figure 4. Architecture of the read-out channel

Illustrative results

Figure 5 shows a photograph and a basic datasheet for the sensor. It also illustrates the system embedding for which the sensor has been conceived. Figure 6 shows a captured image.

References

- [1] A. El Gamal and H. Eltoukhy, "CMOS Image Sensors". *IEEE Circuits and Devices Magazine*, pp. 6-20, June 2005.
- [2] JAI ltd. www.jai.com.

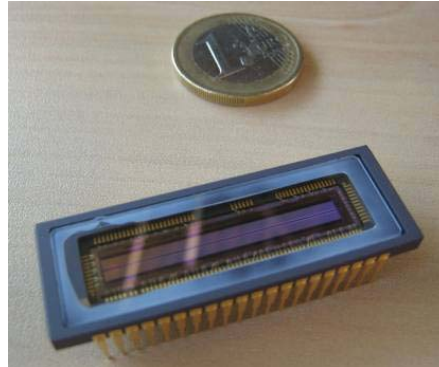


Image sensor		On-chip image processing	
Active imager size	28.91mm (H) x 35μm (V)	-6 to +21dB programmable gain	
Active pixel	3 x 4,096 (standard mode)	±500mV programmable offset	
Pixel size	7μm x 7μm (standard mode) 14μm x 14μm (binning mode)	Vertical FPN (VFPN), PRNU, DSNU and lens shading correction logic	
Pixel type	4T active-pixel with pinned photodiode	Miscellaneous	
Shutter type	Global with programmable exposure time	Package	40-lead ceramic IDK
Line rate	15,000lps (standard mode) 27,000lps (binning mode or sub-sampling) 44,000lps (binning and sub-sampling)	Power supply	Dual 3.3V/1.8V
Dynamic range	70dB	Power consumption	500mW (max)
SNR _{MAX}	47dB	External clock	10 MHz
Saturation exposure	47.6nJ/cm ² (standard mode)	Master clock freq.	70MHz
NEI	13pJ/cm ² (standard mode)	Op. temperature	-30°C to +70°C
Peak response	64V/(μJ/cm ²) (standard mode)		
Image lag	< 1.5%		
PRNU	< 0.2% (with on-chip calibration)		

Figure 5. AFSL4k sensor photography and basic data



Figure 6. Sample image captured by AFSL4k sensor at 15,000lps (only VFPN corrected, no PRNU/DSNU correction is applied)