

Column Fixed Pattern Noise Suppression with STI profile control in 1.75 μ m Pixel CMOS Image Sensor

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Abstract

In small pixel of CMOS image sensors, low light performance is increasingly dominated by the noise characteristics. Under a high gain condition of low light environment, the noise can also be amplified by the pixel signal. And especially, the fixed pattern noise is more unpleasant to human eye than random noise. In order to minimize that noise level, we have focused on the shallow trench isolation (STI) of small geometry transistors in active area (AA) conjunction profile and optimized the structure to improve small device variation. This paper presents the investigation of improving image quality in 1.75 μ m 2mega pixels with 0.11 μ m CMOS image sensor technology by suppression the column fixed pattern noise (CFPN).

I. INTRODUCTION

CMOS image sensors have many merits such as the low power consumption and system-on-chip solution. However their column to column pixel readout scheme causes some variation of image. For circuit designers, it is very important to reduce device variations, which are closely related to noise level and such deviations of pixel transistors or many of switching circuits existing in every pixel column line can induce image degradation. Pixel signal variations are converted into image with noise of column-wise, column fixed pattern noise (CFPN) which limits the quality of low light performance. CFPN have more serious effect on image quality of (4~5 times more) than temporal noise does, and especially, it cannot only be suppressed by circuit design because of column readout operation [1]. CFPN mainly comes from column decoder or column switch block column to column variation which is originated by small geometry transistor's performance distribution [2]. Thousands of CMOS process steps which are used for device integration, originally have their own

parameter range so that device characteristics have no choice but to follow the distribution window and small geometry transistors exhibit more wide performance not easily controlled [3]. Unfortunately, most of circuit blocks are designed by not wide active width/long channel gate poly for speed but small geometry, and chip size issues and pixel transistors are all composed of narrow width geometry. And pixel to pixel output signal uniformity is a very important parameter. In order to investigate the relationship between CFPN and key point of process steps, there need to evaluate test pattern, pixel probe test data and physical analysis. All of test patterns dropped in scribe lane data are closely investigated and their physical analysis will be followed.

II. TEST PATTERN AND PIXEL DATA EVALUATION

In the view of process control, scribe lane test patterns of the 1.75 μ m pitch pixel vehicle contain some typical active width and poly length transistors so as to monitor abnormal process trend or electrical data change. In the initial status of pixel development, we have focused on stack height reduction in pixel area and 1.75 μ m pixel sharing layout optimization. After Sensitivity and saturation of target are achieved, dark defect and transfer efficiency limit the performance so that we have made fine tunes such as the photodiode pinning layer, Tx Tr (transfer transistor) V_{th} adjustment and the annealing in H₂ ambient at the related process. The existing state of image quality is able to cover moderate luminance and zero lux condition. But in the dimly luminance condition, image sensors have to detect object by amplifying pixel signal with high gain and the condition is much tough environment without noise improvement. There needs to evaluate the low light condition at the wafer level with image quality

and pixel bayer data testing under the IP750 test machine was set up at low light condition about 0.1~0.5lux with 10times higher gain of moderate illumination test condition [4]. Under the low light condition, the column fixed pattern noise is to be screened out in wafer level by algorithm that compares averaging code of every column data with neighboring line (line averaging and line by line comparison) and calculated standard deviation of line averaging. From those pixel probe test and transistor monitoring data, we have found out their dramatic relationship with 3.3V NMOS transistor of 0.135/10um[W/L] [Fig.1-a], but typical size of transistors provides us only meaningless data [Fig.1-b]. This reveals the overlap portion of STI edge under poly gate incites threshold voltage (V_{th}) fluctuation by poly bending phenomena at the overlap area. At the abnormal profile of STI to AA edge, as it is called, moat (or divot) profile, the electrical field is more concentrated than channel area and moat depth control is critical point for small geometry devices such as pixel transistor and other many of switching circuits. To confirm the effect of the moat depth on pixel CFPN data, we have checked out gate oxide integrity comb pattern having large portion of STI moat under poly gate, which plays a role of edge area portion and contributes to total GOI capacitance measurement data [Fig.1-c].

III. STRUCTURE ANALYSIS

The pattern of narrow active width and long poly length transistor (3.3V NMOS W/L=0.135/10um) is a good indicator of small geometry transistors of pixel transistor and real column line circuitry because the pattern's large overlapping area of STI edge under the poly gate can amplify the electrical data such as the threshold voltage (V_{th}) change of small transistors or variation enough to detect in circuit level probe test and image evaluation. We select some group of chips and the pixel probe data resulting in "bad" die and "good" die screening them out as the test specification of CFPN code. For getting meaningful result from vertical structure inspection, the "bad" means CFPN code about 5code, and "good" does 2code of CFPN. The cross-sectional view of TEM [Fig.2] in narrow width transistor reveals certain difference of STI edge's moat depth that deeper depth can make small geometry devices more sensitive in their electrical data changes by electrical field concentrating [5]. Gathering up above the threads, we thoroughly investigate the front

end process steps and improve the out front structure for oxide filling at shallow trench by pullback process modification. The result of data plot shows that the small geometry transistors move to slower corner direction except wide width, the typical size transistor keeping up their V_{th} and V_{th} variation reduced of small transistor [Fig.3]. To compare the die of original moat depth and improved die, we have investigated them and confirmed that the improved process gets rid of any moat(divot) profile at the edge of STI. In addition, poly gates of source follower circuit exists unnecessary nitride residues at original STI process, but the new process removes it so that potential yield drop can be prevented from the structure not intended. [Fig.4]. Group of standard cell library composing logic circuits and SRAM bitcell needs to be re-characterized for adjustment of circuit timing and then we achieved final design that makes a low light image performance be free of CFPN yielding stabilized quality of 1.75um pixel production [Fig5].

IV. Result and Discussion

Pixel transistors which organize reset, driver and selection transistor have small geometry active width and poly gate length and a lot of switching circuits do too. In this work, we have improved moat depth of small transistor and confirmed low illumination image with CFPN pixel evaluation of photon transfer curve method (PTC) which shows multiple shots average as the lux variation and standard deviation of column average in pixel test plane. This reveals our final work is much effective method in order to reduce fixed pattern noise level [Fig6].

V. CONCLUSION

In this paper, we have founded out that STI edge moat is the strongly concentrated point of electrical field from gate poly and a slight difference of the moat depth as transistor to transistor, especially small geometry transistor, causes column-wise image variation, that is, column FPN and the experiment of moat depth control result in good image quality with low CFPN value due to the reduction of small geometry transistor variation.

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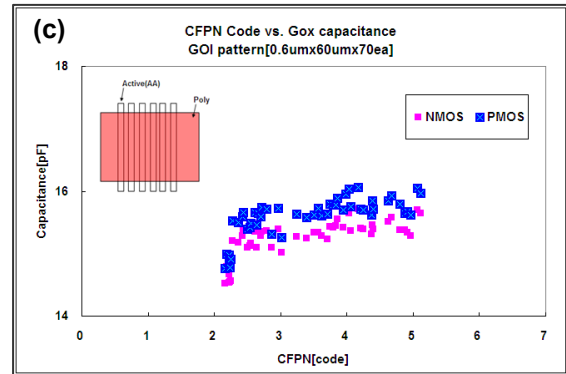


Fig.1: The plot of CFPN vs. transistor data

- (a) narrow active width and long channel,
- (b) typical size transistor (normally checked out),
- (c) GOI pattern of active comb layout

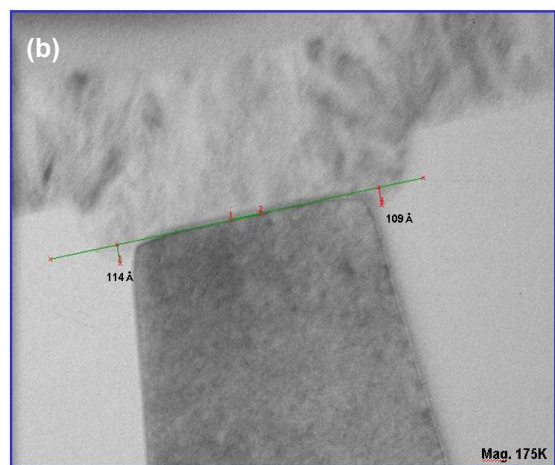
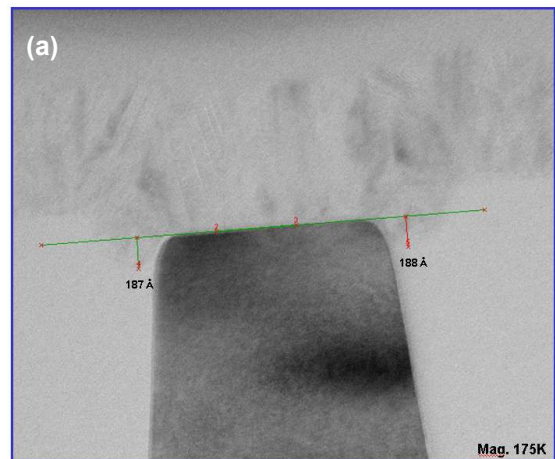
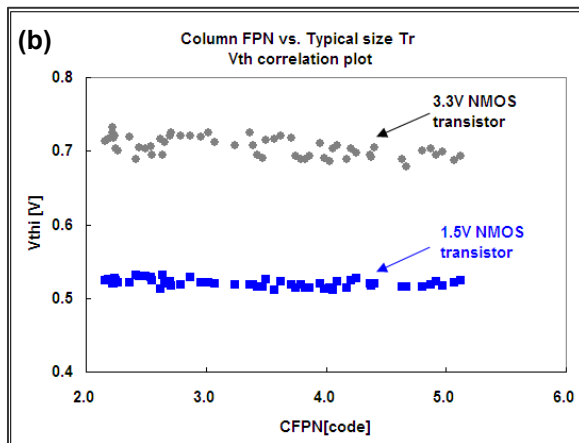
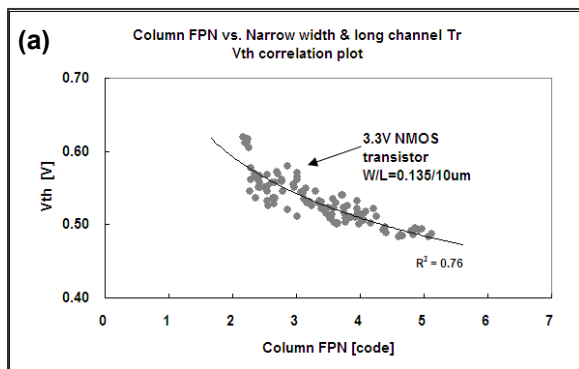


Fig.2: TEM comparison view of STI edge profile

- (a) CFPN "bad (5code)" sample,
- (b) CFPN "good (2code)" sample

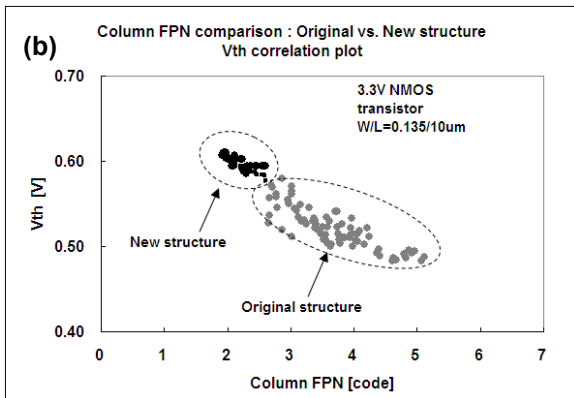
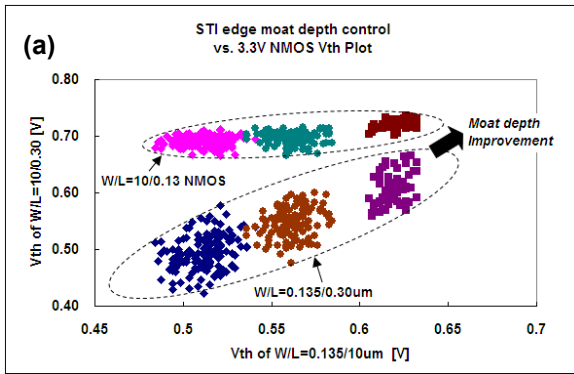


Fig.3: (a) is transistor V_{th} change as the STI moat depth experiment with geometry
 (b) CFPN code comparison original vs. New structure.

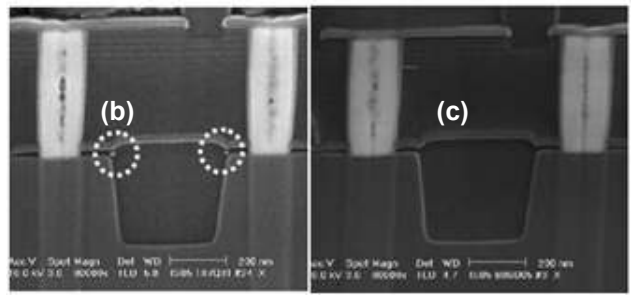
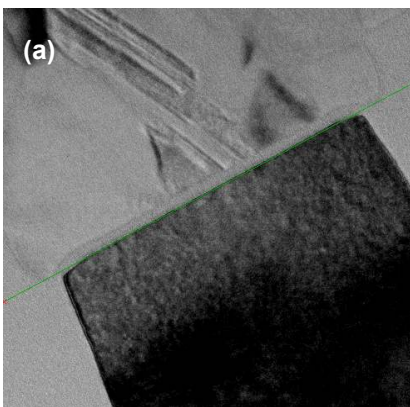


Fig.4: Process improvement results of STI edge moat (divot) depth: (a) New structure shows no divot at the edge of STI
 (b) unnecessary residue @pixel transistors' divot
 (c) new structure clean up all nitride residue.

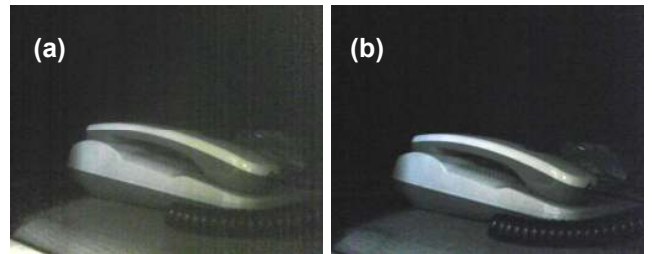


Fig.5: Module image comparison @low light condition
 (a) original image(vertical noise line can be seen)
 (b) CFPN noise improved image.

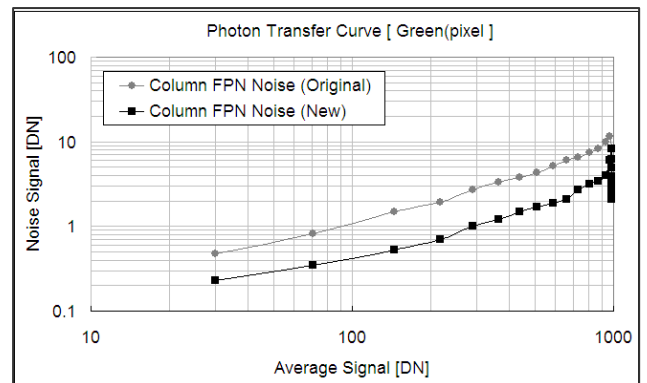


Fig.6: Column FPN comparison: photon transfer curve(PTC) method plot as the luminance variation from low light to saturation. This plot contains 20shot average pixel frame data and standard deviation of all.