400x400 pixel image sensor for endoscopy in 1.7mm^2 CSP package

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This paper describes the challenges related to the design and manufacturing of the smallest, packaged, color sensor in the world. The sensor uses 2.8um pixels implemented using TSMC 0.18um CIS technology to achieve 400x400 resolution in a 1.78x1.78mm Chip Scale Package (CSP). A hybrid (analog/digital) fully differential I/O (patents pending) is capable of driving cables up to 5m long while keeping the total power consumption below 80mW.
To achieve this, every common practice in image sensor design had to be questioned and re-thought in order to achieve the maximum possible area efficiency.
As if the design challenges were not enough, manufacturing constraints contribute in painting a rather complex picture. For example, the distance between active pixels and the dicing lanes has to drop below typical design rules. As a consequence, the manufacturability of color filters and micro lenses needs to be validated. In the same way, the effect of mechanically-induced stress during dicing may now propagate to the first rows/columns of pixels shifting their performance, especially in terms of dark current.

Introduction

The field of image sensors for endoscopy application is still largely covered by the use of CCDs, bundles of optic fibers and, in some cases, just arrays of lenses. Current CMOS and packaging technologies are enabling ultra-small cameras that can be designed into the next generation of endoscopes providing dramatic increase in resolution and performance.

Floorplanning

Designing an image sensor of these dimensions requires a change in the design flow/methodology. Floorplanning is a fundamental step needed to define area budget for each block. Area has to be considered, next to bandwidth, power consumption and Signal to Noise Ratio (SNR), as a critical parameter for the design and definition of each block.

A sketch of the sensor's floorplanning is shown in Figure 1 (note: blocks are not drawn to scale).
There are several restrictions that need to be accounted for when defining the floorplan:
- Wafer-Level Chip-Scale Packaging (WLCSP) requirements
- Signal path uniformity (e.g.: maintain similar tracks for fully-differential signal pairs)
- Routing requirements
- Scalability for a family of product

For these products, rather than X-Y dimensions, the blocks are budgeted based on area requirements, as "rectangular" footprints may not be the most efficient solution.
Area budgeting is also useful to more accurately estimate the trade-off between pixel size and resolution. In typical image sensors applications the area of the image core is fixed, so smaller pixels correspond to higher resolutions. In our case the total area of the image core was fixed. Smaller pixels pitch corresponds to tighter column buffer/amplifiers as well, which, in turn, grow length-wise.
Let's look at a practical example:
- Total area available for image core ~1350x1350um
- Estimated area of column buffer/amplifiers: 600um^2

Scenario #1: Pixel pitch 2.8um
- Length of column block: 600/2.8 = ~215um
- Corresponding resolution: (1400-215)/2.8 = ~405

Scenario #2: Pixel pitch 2.2um
- Length of column block: 600/2.2 = ~275um
- Corresponding resolution: ~488
- Corresponding resolution in case of fixed array size: 405*2.8/2.2 = ~515
- Delta due to scaling of column buffer: ~30 pixels

Manufacturability and reliability of the sensor are especially critical on medical devices. Best Known Methods (BKM) are not necessarily applicable at these dimensions or may no longer be sufficient: for this reason, special care has been taken in defining specific design rules that reduce the risk of performance degradation due to mechanical stress.

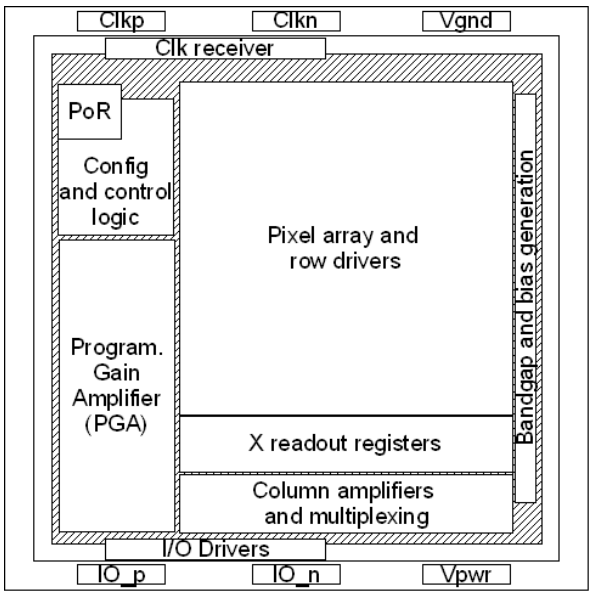
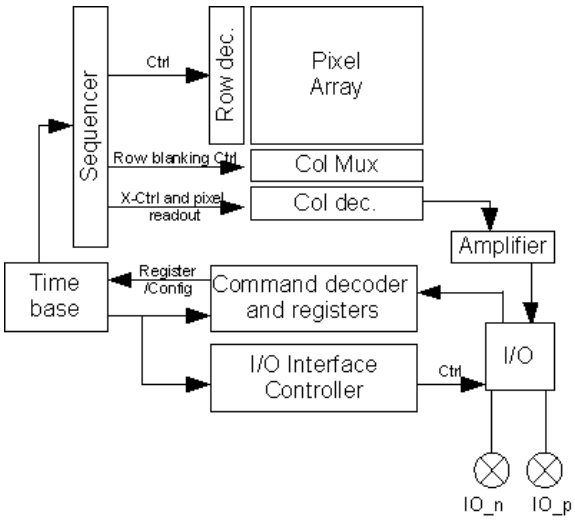


Figure 1 Example of floorplanning.

Image Sensor Design

The architecture of this sensor with an effective resolution of 400x400 pixels is described in Figure 2. Black level calibration is performed in the PGA by using an electrically generated reference which eliminates the need for optically black pixels. The analog output is fully differential to maximize SNR in a noisy environment.



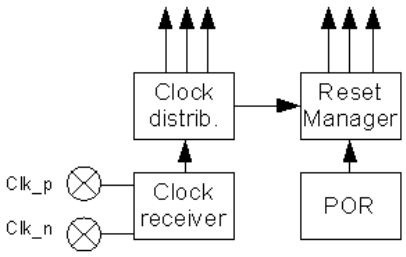


Figure 2 Block Diagram.

The entire sensor operation relies on proper reset triggered by an on-chip Power-on Reset (POR) circuit that ensures correct startup and initialization of the sensor. The sensor starts acquiring images once the power supply is stable and all biasing conditions are met.

The most innovative feature in this sensor is the I/O control (figure 2). This sensor employs a hybrid digital / analog and bidirectional I/O which allows precious area saving deploying only two bond pads (patents pending). The single I/O interface is used for analog image data output, synchronization signal output and as a configuration interface.

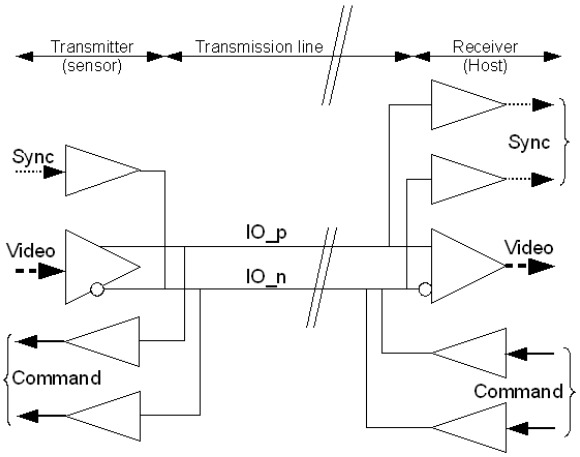


Figure 3 Functional diagram of the Synchronization/Video/Command bidirectional link.

The I/O has to be able to function in these three modes without requiring explicit hand-shaking protocols, to limit the pin count and interfacing complexity. For this reason a fixed frame format has been developed in which the three types of data are time-multiplexed (Figure 4).

A frame denotes a period of time during which one image is transferred. Besides image data, a part of the frame time is spent in overhead time (frame blanking, line blanking) and extra timeslots to facilitate system synchronization information and to provide a mean to configure the sensor.

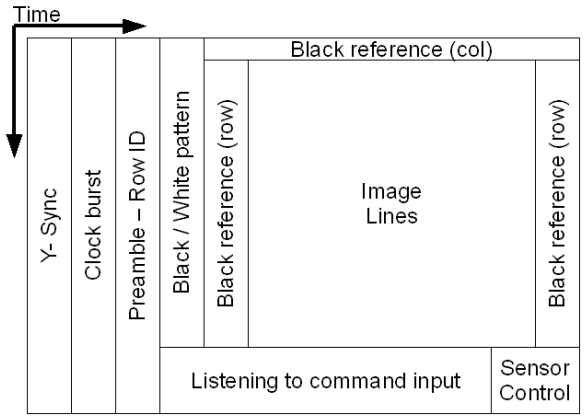


Figure 4 Frame Format. Time evolves from left to right, top to bottom.

When sensing out analog image data, the output signal is fully differential. The common mode is at a constant level. Synchronization data is sent by switching the common mode level high or low (figure 4). Such separation is required to enable the host to differentiate between the two types of output signaling.

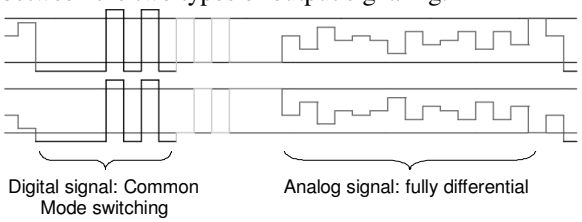


Figure 5 Level separation between analog and digital.

In the frame format (Figure 4), a dedicated timeslot is foreseen to upload configuration data such as gain, frame and exposure parameters to the sensor. This timeslot is announced by the sensor by sending out a specific synchronization pattern.

During the upload timeslot, both I/O pins are driven to the logic high level before being tri-stated. An upload can then occur by applying a clock signal to one of the I/O pins and the data to the other I/O pin. If no upload is required, the pins stay in high-Z mode. Weak pull-up resistors will then keep both I/O lines high. The control logic will take care of interpreting the commands and executing them in the next available frame: this may be the frame immediately following the upload or the successive one, depending on the nature of the new command. For example, a change in the integration time will require a modification of the number of dummy lines.

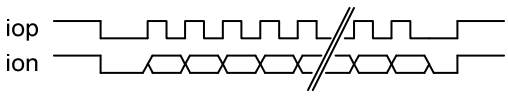


Figure 6 Illustration of a command upload protocol

Packaging

The only sensitive choice for packaging on ultra-small devices is Wafer-Level Chip-Scale Packaging (WLCSP).
WLCSP guarantees that the final dimensions of the devices are substantially coincident with the dimensions of a single die, however, they may also introduce restrictions to the floorplan.

The typical solution for image sensors consists in building a cavity over the image array. This is achieved by building "cavity walls" or "spacers" around the edges of the sensor which separate the glass from the surface of the sensor (see Figure 7).
To prevent covering active pixels with the walls, a minimum space of about 350~400um is required between the edge of the chip and the first active pixel. This would have reduced the available area for active pixels and required it to be placed in the middle of the sensor.
For these reasons a solution without cavity was preferred.

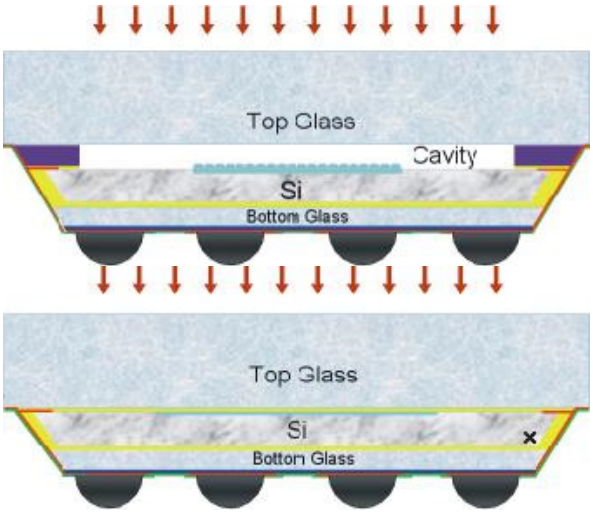


Figure 7 WLCSP with (top) and without (bottom) cavity – courtesy of Tessera (www.shellcase.com)

This posed yet another technical challenge: how to maintain the effectiveness of the microlenses (a must for 2.8um pixels) and the glue. The solution consisted in coating the microlenses with a material with an appropriate index of refraction.

Limiting factors

Despite the use of WLCSP solution without cavity, the package is still the limiting factor for further scaling the sensor. The BGA on the back of the sensor infact is at the limit of current mainstream process capability. Options are being explored to overcome such limitation.

Conclusions

In this paper we presented an ultra-small, 400x400 pixel sensor designed for endoscopy applications. By designing a hybrid analog/digital I/O we've been able to maintain a low pin-count without sacrificing functionality. Manufacturing solutions have been found to eliminate the need for cavity walls which allowed maximum area efficiency.

The modular design allows easy scalability for easy implementation of a family of products

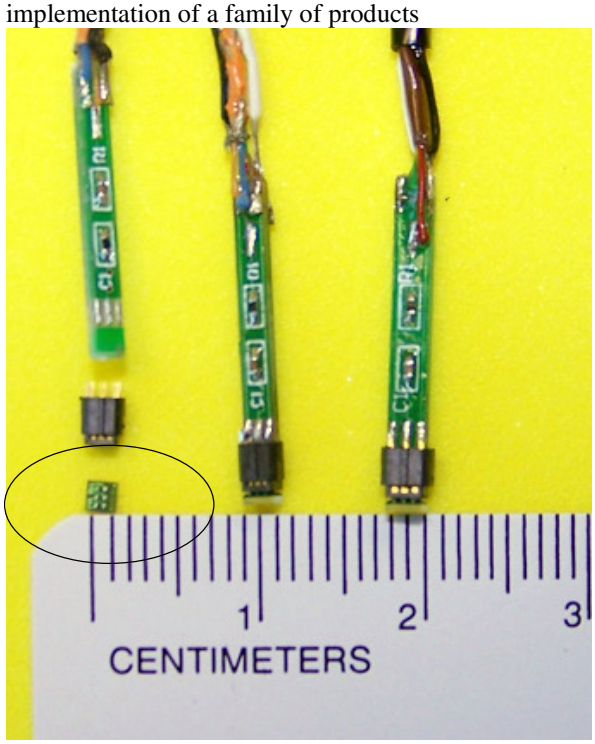


Figure 8 A family of 3 sensors (400x400 on the left) already connected to the tips of endoscopes[1]

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References

[1] J. Adair, "Medical Image Sensors", ISSCC 2009, San Francisco, CA, March 2009