

A High Speed Pipelined Snapshot CMOS image sensor with 6.4 Gpixel/s data rate

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This paper describes a high sensitivity, high speed CMOS image sensor, implemented in a 0.18 μm CMOS process. The sensor runs at 6242 fps for a maximum frame size of 1280 x 800. This results in a data throughput of 6.4 Gpixel/s. By reducing the window size to 128 x 8, the frame rate can be boosted to no less than 1 Mfps. In order to increase the parallelism the sensor architecture is composed such that it actually merges 2 sensors of frame size 1280 x 400. These two sub-parts are read out simultaneously on opposite sides of the die, which is about 29 x 25.5 mm^2 . The die size was maximized to allow for a pixel size of 20 x 20 μm^2 , resulting in a high responsivity of 13100 $\text{V/s}/(\text{W}/\text{m}^2)$ @ 550 nm and a DR of 63 dB. The pixel type is 6T-based which is capable of pipelined, snapshot shutter operation. The image core output is multiplexed to 128 Analog Front End (AFE) channels, each operating @ 65 MSamples/s. Total power consumption is 2.5 W for a 3.3V power supply.

Introduction

For a high-speed image sensor, in general both the light sensitivity and obviously the frame rate are the most important specifications to focus on. The light sensitivity is mainly determined by the physical aspects of the silicon (QE), the pixel size and conversion gain. These are properties that are mostly dependent on the pixel design and choice of technology. The frame rate on the other hand can be improved in two ways. Where in the past, the focus was set on increasing the readout speed and reducing the overhead times, currently the attention is somewhat shifting to an increase in parallelism. Despite the technology scaling, the ability to improve the signal transfer times is being limited by the physical dimensions of the sensor.

Image sensor design

Figure 1 is showing the sensor architecture. The pixel array is operated globally by the pixel drivers, but the column outputs are split for top and bottom parts. The column structure buffers the pixel output and drives the signal to the AFE, which brings the analog signal off-chip with a final output swing of 1.3 V. The sensor timing is system controlled in order to allow for maximum flexibility in trading readout speed for image quality.

The on-chip x-shift register can be given an address pointer in order to reduce the window size and boost the frame rate. The y-shift register on the contrary always starts readout from the center of the chip. A 16 bit addressable SPI interface is used to program the start address pointer, bias settings and other programmable sensor functionality.

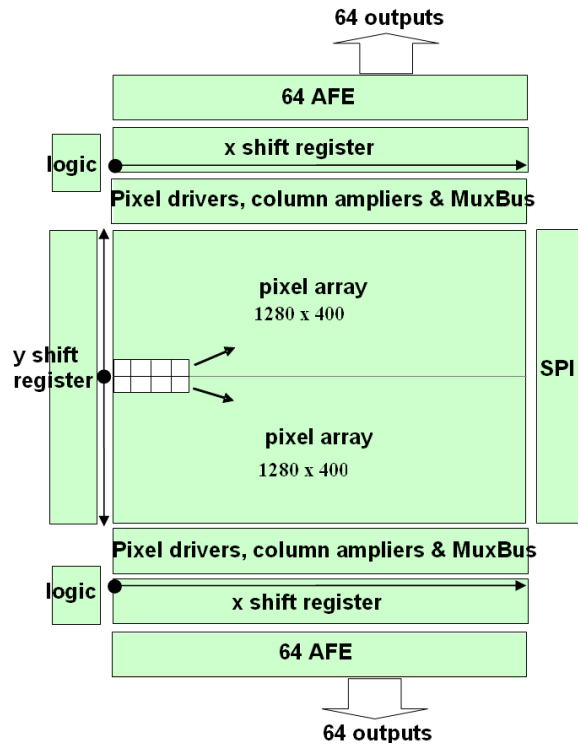


Figure 1 : Sensor architecture

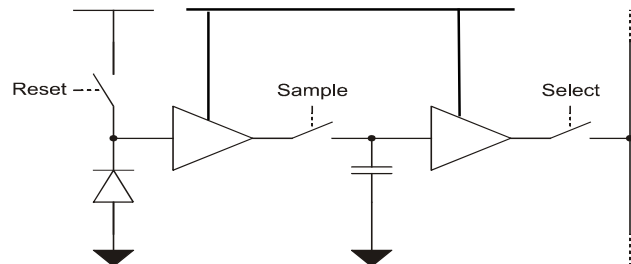


Figure 2 : 6T pixel architecture

The image core is the main design bottleneck to optimize for high speed operation. Power supply routing and block partitioning are key issues to minimize frame blanking and row blanking times and to achieve the required channel speed.

The 6T pixel (Figure 2) actually has 2 supplies which separate the diode part from the storage part. This makes sure that the diode in pipelined operation is not influenced by any power supply noise during readout which enables exposure times down to 300 ns. The sensor also incorporates an Anti-Blooming feature and a dual slope mode to increase Dynamic Range (DR). The pixel size (20 μm x 20 μm) is large enough to select 4 rows simultaneously in each half without sacrificing a lot of Fill-Factor. This reduces the amount of row blanking times by a factor 8 compared to a single row select in a progressive scan sensor. The implemented kernel size is therefore 16 x 4 in each half.

The column structure has a lot of flexibility with respect to sampling modes and current loading. Optional column Sample-and-Hold capacitors can be used to reduce the row overhead time and to shield the pixel column lines from the stored line values being read out. This feature facilitates the exposure start timing without inducing reset line artifacts.

The column amplifier is optimized to drive the large multiplex bus structure which uses precharging to avoid horizontal ghosting. Because of this 'reset' behaviour of the amplifier load, an n-type source follower is best suited to charge the bus load quickly. This source follower is preceded by a p-type source follower and a one-stage differential-pair amplifier. High-Speed sensors of the past used to cascade these building blocks. For this sensor, the amplifier architecture was adapted to significantly improve the signal attenuation along the analog path and reduce the amount of column non-uniformity by including the source followers in the complete amplifier feedback loop (Figure 3). The amplifier architecture is kept deliberately simple because of the severe layout constraints (5 μm pitch, 3 routing metals) as well as to minimize the total power budget (700 mW for the imagecore). A lot of care has been taken to define a deterministic state of the amplifiers' internal nodes during idle time in order to avoid any row crosstalk.

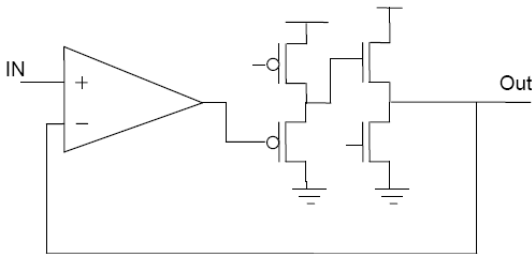


Figure 3 : Column amplifier

The multiplex bus structure is the interface to the AFE. It implements the increased frame rates in windowing mode and poses the main physical limit on channel speed. Two different sets of busses are operating at half the channel speed while being shifted 180° out of phase in time. Finally the AFE multiplexes 2 time-shifted bus signals to generate the full-speed output signal.

A lot of design effort was invested into the multiplex bus structure layout in order to present a balanced load to the column amplifiers. Due to the large amount of sensor outputs, the total bus structure is containing 128 busses which takes about 1.3 mm in width. This size is enough to significantly increase the RC-time constant for the bus with the topologically largest distance from the column amplifier. The reason is a not to be neglected increase in interconnect resistance before reaching the largest capacitive load which is the bus itself. A total difference of 40% in settling time was seen between the nearest and the most distant bus. All busses were carefully balanced in layout resulting in a difference of only 1% in settling time over all the busses which improves kernel uniformity and relaxes the slewing current needed for the column amplifiers.

Where the AFE's main purpose is to multiplex the two bus sets and drive the signal off-chip @ 65 Msamples/s, it also incorporates an optional Sample-and-Hold stage, and the ability to multiplex the kernels to only 64, 32 or 16 of the outputs, thereby reducing the frame rate and power consumption drastically.

The silicon is packed in a 314 pins PGA package with built-in peltier cooler (Figure 4). This cooler is capable of transferring a minimum of 11W of heat power which is sufficient to keep the die temperature stable.

Considerable of attention was paid to the package design as well. Implementing a low-ohmic connection for all the power supplies including the sensor ground is critical considering the total power consumption and the large peak currents of the sensor.

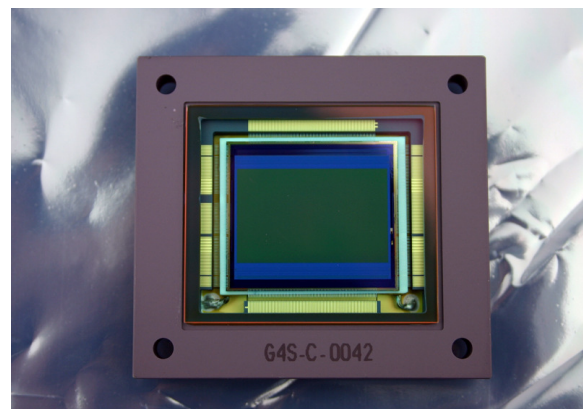


Figure 4: 314 pins PGA package with built-in peltier

Experimental results

Full characterization has been finalized and the product is ready to be released for full production. An offline corrected color image is shown in Figure 5.

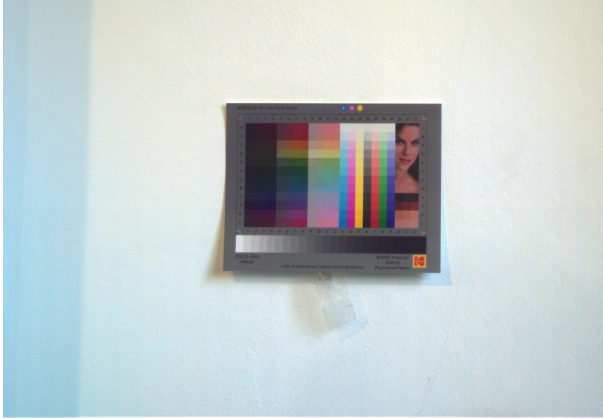


Figure 5 : Full frame color picture of the sensor with offline correction

The key sensor specifications are listed in Table 1.

Parameter	Value	Remark
Pixel size	20 x 20 μm^2	
Pixel array	1280 x 800	
Pixel type	6T	Pipelined, snapshot shutter
Interface	Analog Out	1.3 V swing
Frame Rate	6242 fps	For full frame readout
Data Rate	65 MSamples /s	
Main power supply	3.3 V	
Power consumption	2.5 W	
Fill Factor	58 %	
Full well	38 ke^-	
Read noise	28 e^-	In the dark
Responsivity	13100 $\text{V/s}/(\text{W}/\text{m}^2)$	@ 550 nm
Conversion gain	32 $\mu\text{V}/\text{e}^-$	@ the sensor output
DR	62.6 dB	Intra-scene
MTF	> 60%	@ Nyquist frequency
FPN	2.9 %	rms of full output swing
RNU	3.1 %	rms of signal level
Dark Signal	85 mV/s	@ room temperature
Chip size	29 x 25.5 mm^2	
Maximum output load	10 pF	
Package	314 pins PGA	With built-in Peltier cooler

Table 1 : Key sensor specifications

Conclusion

This paper presents the development of one of the highest speed image sensors. The key aspects for the sensor and package design have been explained. The use of an attenuation-free column amplifier and balanced-load multiplex bus structure has been proven critical to support the high frame rate without losing too much of signal swing and conversion gain. A lot of flexibility with respect to readout modes has been implemented in order to squeeze the maximum performance out of the part. To build a successful camera with this high-speed sensor, attention must be paid to similar issues as described in this paper on system level. Minimizing the output load to 10 pF and equalizing the interconnect properties for all outputs is very important in order to reliably sample the analog output signal and achieve a good image quality.