An advanced CMOS Active Pixel Sensor in a novel quadruple well process (INMAPS) for 100% Fill Factor and Full CMOS Pixels

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Abstract

In scientific applications it is often required to have signal processing in the pixel. As the diode is normally formed by an N implant in the P-doped epitaxial layer, the use of PMOS transistors in the pixel is prevented if high collection efficiency is desired. In order to overcome this problem we developed a CMOS process (INMAPS) with a deep P-well implant that can be used to surround N-wells wherever needed. This novel quadruple well process was used for the manufacturing of an advanced CMOS Active Pixel Sensors designed for use in an electromagnetic calorimeter, one of the detector subsystems in a particle physics experiment. The main characteristics of the sensor as well as experimental results are presented here. The efficiency of the quadruple well is also demonstrated.

Design

The cross-section of a standard CMOS wafer is shown in figure 1. In most image sensors the junction between an N-well or equivalent N implant and the P epitaxial layer is used to form the detecting layer. This structure provides high charge collection efficiency [1]. High-energy charged particles, which are commonly to be detected in particle physics experiments, can traverse metal structures and deposit a uniform trail of energy in silicon, generating about 80 electron-hole pairs in every micron of silicon they traverse. So effectively the N-well to P-epi diode gives 100% fill factor for the detection of charged particle[2], but only if no PMOS transistor is used in the pixel. This severely limits the use of CMOS sensors in this kind of experiments as well as in other scientific application as in-pixel processing is needed. In order to overcome this problem, we developed a quadruple well process (INMAPS) adding a deep P-implant in an advanced 0.18 μm CMOS technology.

Using this process, we have designed a number of sensors, and the first application was for a CMOS sensor (TPAC [3]) for an electromagnetic calorimeter[4] for an experiment

[1] B. Dierickx, G. Meynants, D. Scheffer, *Near 100% fill factor CMOS active pixels*, 1997 IEEE CCD & Advanced Image Sensors Workshop, Brugge, Belgium
[2] R. Turchetta et al., *A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology*, Nucl. Instruments and Methods A (2001), 120-129
[3] TPAC stands for Tera-Pixel Active CMOS sensor, as the total number of pixel in the electromagnetic calorimeter is about 10^{12}
[4] M. Stanitzki et al., *A Tera-Pixel Calorimeter for the ILC*, Proceedings of the IEEE Nuclear Science Symposium, Hawaii, USA, November 2007

at the future Linear Collider[5]. The pixel pitch is 50 μm and the arrival time of every charged particle needs to be recorded with a resolution of a few hundreds ns.

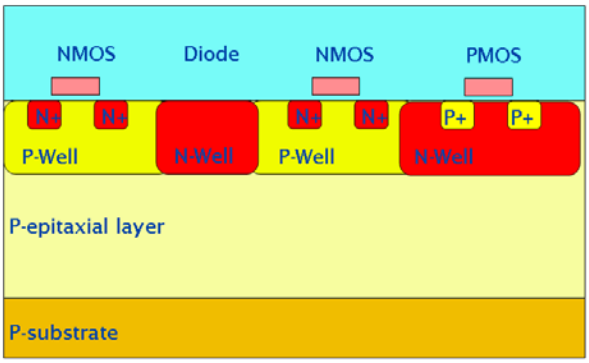

Figure 1. Schematic cross-section of a typical CMOS wafer. Not drawn to scale.

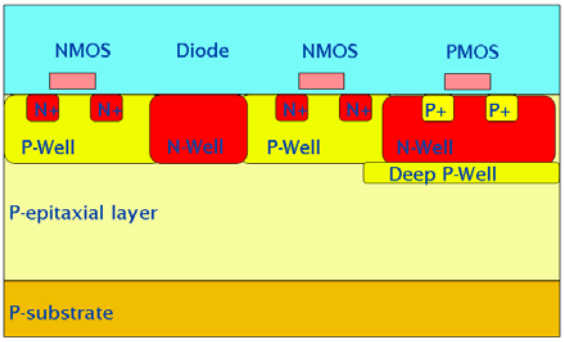

Figure 2. Schematic cross-section of a CMOS wafer with the deep P-well implant (INMAPS process). Not drawn to scale.

In this prototype we manufactured sensors with 5 and 12 μm thick epitaxial layer, the former being the standard thickness for image sensors and the latter being better optimized for the application as the signal is proportional to the thickness of the layer. As the collection is mainly by diffusion, we estimated that the most probable signal generated in a pixel is about 400 e- in the thicker layer. The main characteristics of the prototype sensor are shown in table 1.

We designed two different pixel schematics, with similar functionalities but different front-end analogue processing electronics. The in-pixel processing chain for one of those, called preShape, is shown in fig. 3. In the other variation, the preSample (not shown), the charge amplifier and shaper are replaced by a more conventional image sensor architecture with a source follower and a sampling circuit. Fig. 4 shows the layout of a pixel, with 4 collecting diodes and deep P-well to screen the N-well of the PMOS transistors. As a total, over 150 transistors are integrated in the pixel, with a roughly equal number of P- and N-MOS plus some other passive components.

Parameter	**Value**	**Unit**
Format	168 x 168	Pixels
Pitch	50	μm
Noise	22	e- rms
Saturation signal	3000	e-
Time resolution	300	ns

Table 1. Main characteristics of the TPAC sensor

The sensor (fig. 5) is organized in eight blocks of 42 columns and 84 rows. The sensor is about 1 cm^2 in surface, with 8.2 million transistors and was fabricated with and without the additional deep P-well. This allowed us to measure experimentally the improvement in charge collection as well as to compare with detailed device simulation. In order to verify experimentally the simulation results we used a pulsed IR laser at 1064 nm with a 2μmx2μm square spot. This wavelength was chosen as the sensor was illuminated from the backside and silicon is transparent at this wavelength, so that charge is deposited in the epitaxial layer. As the pixels in the array do not have any analogue output, the signal amplitude was determined with a threshold scan (fig. 6). In order to align the

[5] LDC Detector Outline Document, http://www.ilcldc.org/documents/dod/outline.pdf
SiD Detector Outline Document, http://hep.uchicago.edu/~oreglia/siddod.pdf

sensor, plots like the one shown in figure 7 were used.

Figure 8 and 9 show the experimental and the simulation results. Both sensors with and without the deep P-well implant are considered. Line F (fig. 4) shows the charge collection efficiency in a line that crosses the center of the pixel. If no deep P-well is present, the charge collection efficiency is very poor because most of the charge is collected by the N-wells where PMOS transistors are created. With the deep P-well about 40% of the generated charge is collected, the rest being collected by neighbouring pixels.

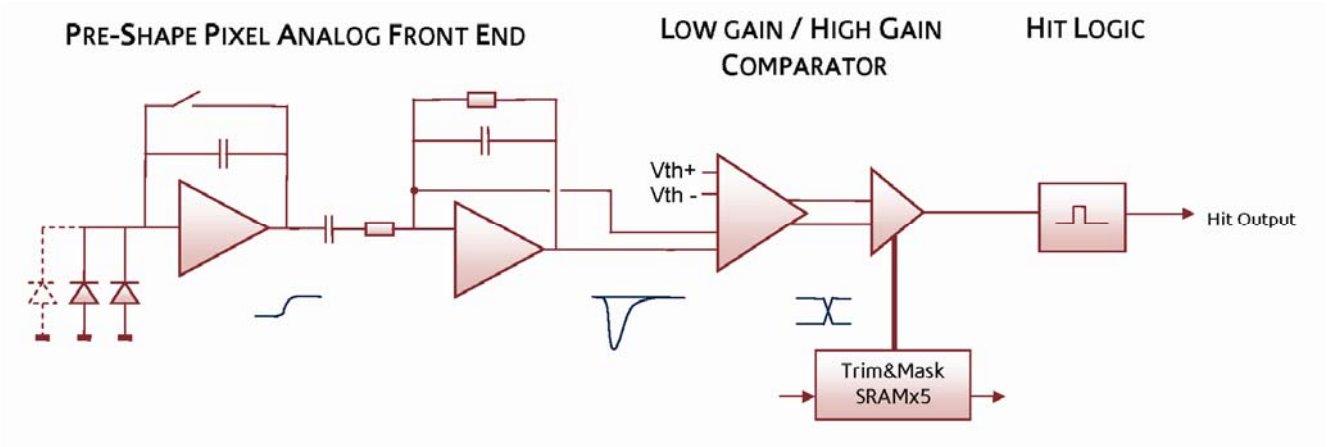

Figure 3. *PreShape* pixel block diagram showing the analogue signal path from collecting diodes to binary *hit* output.

Figure 4. Layout of a *preShape* pixel from the TPAC1.0 sensor. Only the N-well (purple) and deep P-well (grey) layers are shown. Every N- well but the detecting diodes have got deep P-well underneath. The non-physical boundary between pixels is shown as a dotted line.

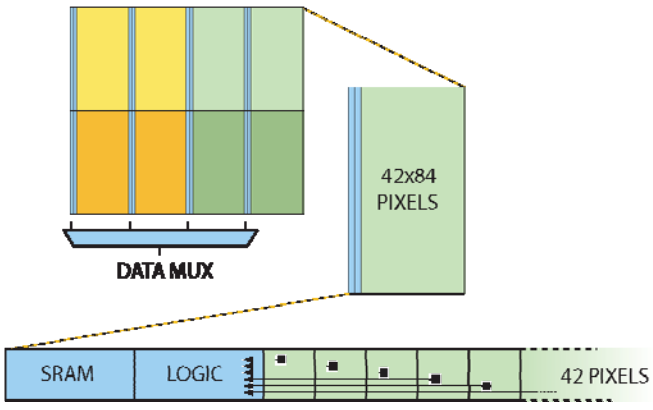

Figure 5. TPAC1.0 sensor floor plan diagram.

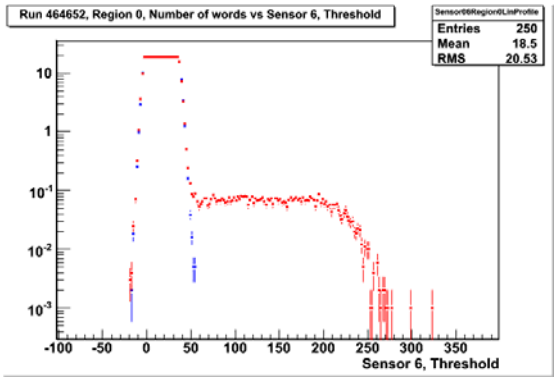

Figure 6 Two typical threshold scan results: (red) with laser source and (blue) without.

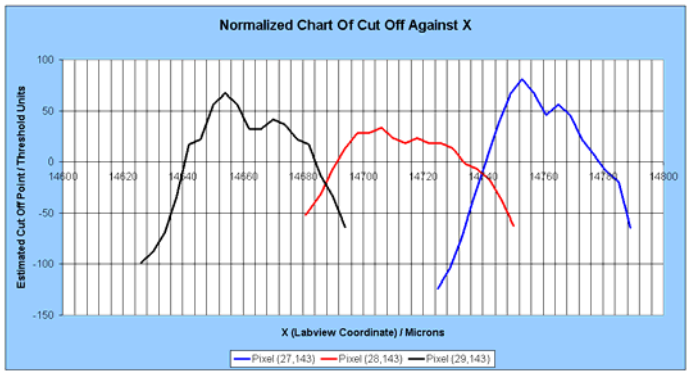

Figure 7. Normalised signal magnitude plots for three adjacent pixels, as used to identify exact location and orientation of sensor when illuminated from the rear surface.

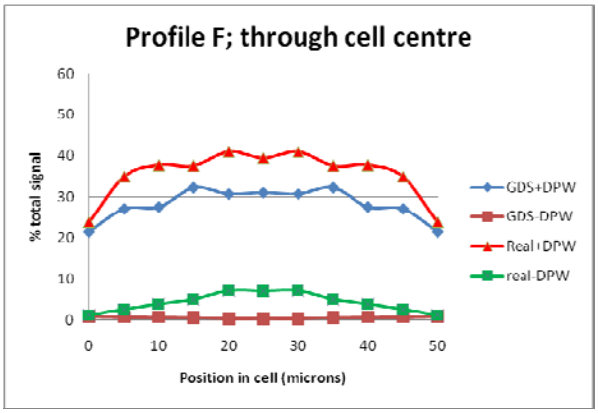

Figure 8. Comparison of simulation results ("GDS") with measured ("real") response of single pixels in array for linear profile F (fig. 4).

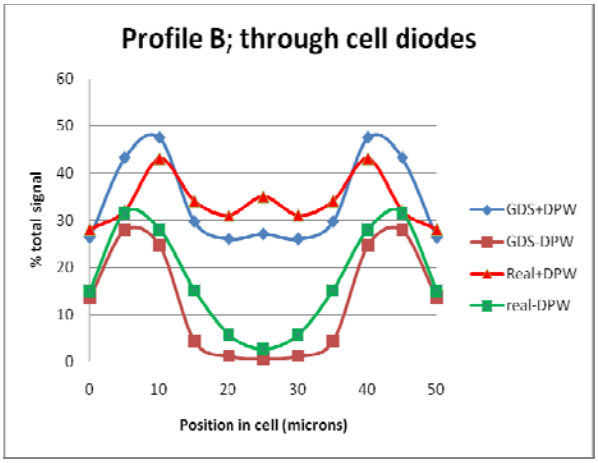

Figure 9. Comparison of simulation results ("GDS") with measured ("real") response of single pixels in array for linear profile B (fig. 4).

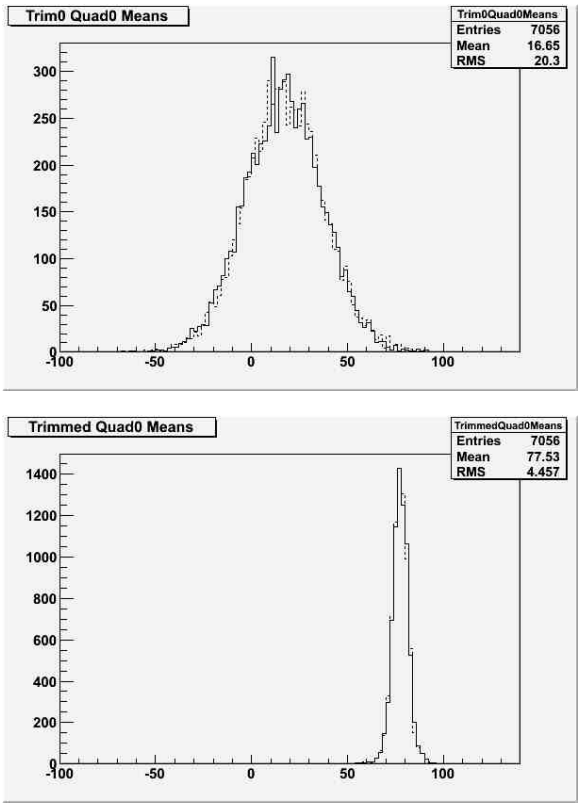

Figure 10. Histogram of per-pixel threshold scan mean values for quad 0 (solid) and quad 1 (dashed) preShape array pixels. Top: before trimming, Bottom: after trimming.

Across profile B, the charge collection in the case of no deep P-well is relatively good when the particle hits the sensor close to the diode but quickly drops to about zero in between diodes. As before the deep P-well ensures a much more uniform charge collection.

In order to address the pixel-to-pixel non uniformity, we integrated a trimming DAC in each pixel. The effect of the trimming over the threshold dispersion is illustrated in figure 10. These results were obtained with the first version of the sensor, where the trimming DAC has 4 bits. Although going in the right direction, the adjustments were not sufficient and in a second version of the sensor we extended the DAC to 6 bits.

The sensor is also currently (April 2009) being fabricated on a substrate with a high resistivity epitaxial layer, of a thickness of 12 and 18 μm. With the chosen characteristics of the substrate, an electric field would be present in most of the sensitive volume thus further improving the charge collection by reducing the lateral cross—talk in the pixel.