

Effects of Negative Bias Operation and Optical Stress on Dark Current

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Abstract—A negative bias operation of transfer gate has revealed a major origin of dark defects of CISs. It has been observed a strong visible light causes a damage of increasing dark current on normal operating condition and anneals the damage in power-off mode, which indicates the strong light possibly causes a threshold voltage shift and that is explained by photon-assisted tunneling or emission mechanisms. Charge injection from photodiode to substrate at the negative bias operation was avoided by an improved well structure.

I. INTRODUCTION

Recent CISs adopt pinned photodiodes with transfer gates, which enable low dark current and true CDS operation. However, to reduce white defects at dark is still challenging. It has been understood that a transfer gate edge and a STI edge of the pinned photodiode are main origins of dark current [1,2,3,4]. In the transfer gate, it is a trade-off to enhance P-well concentration below the transfer gate because it improves the dark current but worsens image lag and charge injection at saturation [5,6].

Negative bias operation of the transfer gate (TG) is a promising method to reduce dark current [6,7]. We have developed a low noise CIS and precisely measured effects of the negative and positive bias operations of TG on sensor characteristics. The results show dark defects of middle level are attributed to the transfer gate. We discuss the reason by using device simulation.

Furthermore, we have analyzed effects of strong visible light on dark current. The results show that the light on normal operating condition causes a damage of increasing dark current, and the damage is annealed again by the light in power-off mode. We discuss the mechanism.

Negative bias operation of TG may cause charge injection from photodiode to substrate. We have introduced an optimized well structure below the TG. As the result, the injection was avoided. We also discuss the reason based on the device simulation.

II. MEASUREMENT

The device we have measured is a 5.6 μm pixel, 640(H) \times 428(V), 4-Tr based pinned photo-diode active pixel sensor [8]. Low level voltage of the TG was varied from +0.5V to -0.7V. Firstly, dark signals of all pixels were stored for 12 sec at room temperature and the differences of dark signals among conditions of TG were measured from cumulative plots. Next, a sensor face plate was irradiated by a strong visible light on several driving and power-off conditions. The light source was white LED, whose wavelength is from 400nm to 800nm, and intensity on the sensor

plate was about 40,000Lux. Finally, charge injection from photodiode to substrate over saturation condition was examined by measuring transfer curves of the sensor at short exposure shutter mode.

III. RESULTS AND DISCUSSION

A. Negative and Positive Bias Operation

Fig. 1 shows dark signal distribution of all pixels on negative TG bias conditions. It is clearly seen that the negative TG operation reduces the number of small and middle level white defects. Only -0.3V is sufficient for the effect. In other words, small and middle level defects are mainly attributed to the transfer gate edge.

Fig. 2 shows results of another device by changing TG bias from positive to negative. On positive TG bias condition, dark signals increase over the whole range.

Potential profile under the TG is simulated on several TG bias conditions using SPECTRATM software. Fig.3 shows the result. From the figure, depleted area under the TG vanishes when the TG bias reduces below -0.3V. It means a surface generation of the dark current reduces, and coincides with the result of Fig.1. On the contrary, the positive bias such as +0.5V makes the surface below the TG widely depleted, which causes a large surface generation.

B. Optical Stress

Fig. 5 shows the effect of optical stress on several driving conditions of TG, where Lo St, Hi St and Nor St designate that TG is held to GND, Vdd and normal operating condition, respectively. Vdd is fixed to 3.3V. In addition, a floating diffusion (FD) node is biased to Vdd. Irradiation period is 10 min. All cases show increase of dark signals; ΔI_d , and it indicates the following relation.

$\Delta I_d (\text{TG:GND}) > \Delta I_d (\text{TG:Normal}) > \Delta I_d (\text{TG:Vdd})$
Comparing Fig. 5 to Fig. 2, the increase of dark signal probably comes from a negative shift of threshold voltage (V_{th}) of the TG.

Negative V_{th} shift is caused by high energy photon [9] or impact ionization [10]. In both cases, holes trapped in gate oxide near Si-SiO₂ interface cause this V_{th} shift, where the holes are generated by high energy photon in the former case or injected from Si by impact ionization in the latter case. In our case, however, photon energy is from 3.1eV to 1.55eV and it cannot generate electron-hole pair in SiO₂. Furthermore, Vdd is 3.3V but the hole barrier V_B from Si to SiO₂ is 3.8eV, therefore, accelerated carriers cannot exceed the barrier height.(See Fig. 6)

As shown in Fig. 7, incident photons generate

electron-hole pairs in FD drain region of Si and photon energy $h\nu$ over band gap energy E_G makes some holes hot. Before cooled by phonon emission, the hot holes reach the surface under the TG, where oxide barrier reduces by $\Delta\Phi_s$; band bending from the drain [11]. Remaining barrier for holes is expressed as $\Delta V_B = V_B - \Delta\Phi_s - (h\nu - E_G)$. When ΔV_B is positive and small, holes subsequently tunnel into SiO_2 through a triangular barrier caused by field $F(x)$ of SiO_2 . When ΔV_B is negative, holes are directly injected to SiO_2 . The former is photon-assisted tunneling [12] and the latter is photon-field-assisted emission. (It was called as photoemission [13,14] when photon is solely related.) Some part of injected holes are captured by trap states, which cause negative shift of V_{th} .

When the TG is GND and the FD drain is Vdd, $F(x)$ or $\Delta\Phi_s$ is large so that a tunneling or a photoemission is much increased compared with the case that the TG is Vdd (See Fig. 4). This results in larger injected charge, and coincides with the differences in Fig. 5.

C. Annealing Effect

We have observed the optically stressed device was annealed by two methods, one was irradiation of strong light, and the other was long time room temperature storage, both were in power-off condition. Fig. 8 and Fig. 9 show those results, respectively. Fig. 9 shows the long time more than 3.5 days were needed to recover to the initial level, but from Fig. 8, only 10 min optical stress was enough to the recovery. The annealing effect for the trapped holes is explained by two mechanisms, one is tunneling and the other is thermal [13]. But in our case, photon is related. As shown in Fig. 10, photons of visible light can stimulate the trapped holes to be emitted [14], which is faster than thermal emission at room temperature, though the rates depend on their trap levels in both cases. For the former case, it may be called as photon-stimulated annealing.

These optical stress and annealing effects are important because the stress causes burn-in effect when strong light is captured and then low light scene is imaged. To relieve the effects, bias voltage of FD node should be reduced during photo-integration period.

D. Overflow at Negative Operation

Negative bias of TG causes a reduction of channel potential and may cause a charge injection from photodiode to substrate at saturation. This phenomenon is observed as a non-linear characteristic in shutter mode operation, because neighboring rows are fully saturated even when a read row is below saturation. (See Fig. 11)

We have modified a transfer gate structure in which P-well concentration of half side away from photodiode (PD) is reduced. A potential simulation of the structure is shown in Fig. 12 comparing with a

conventional one. Fig. 12 (b) shows that a charge spilling path of the structure is formed not at the interface but in the bulk region, therefore, this path is not closed when the gate bias is reduced to negative. Fig. 13 shows transfer curves of the sensor at short exposure shutter mode on several bias conditions. Even on -0.7V, non-linearity is not observed over Po, the light intensity where the PDs of the adjacent rows are saturated. Fig. 14 shows a comparison of the transfer curves between short exposure shutter mode and full frame mode, where a horizontal axis is calibrated with integration time. Sensitivity is strictly proportional to the integration time that means there is no charge injection. A slight offset in shutter operation is caused from image lag but the difference is only 1 LSB of 13-bit (2 e-).

IV. CONCLUSION

In this work, we have evaluated the effects of negative and positive bias operations of TG on dark signals, and revealed a major origin of the dark defects of CISs. Strong visible light causes a damage on operating condition and anneals the damage in power-off mode, which should be attributed to photon-assisted tunneling or emission and photon-stimulated annealing mechanisms. A charge injection from photodiode to substrate at the negative offset operation was avoided by an improved well structure.

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REFERENCES

- [1] H. I. Kwon et al., IEEE Trans. Electron Devices, vol.51, pp.178-184, 2004.
- [2] B. Pain et al., IEEE Workshop on CCDs and AIS, pp.145-148, 2005.
- [3] Y. Kunimi and B. Pain, Int. Image Sensor Workshop, pp.66-69, 2007.
- [4] C-R. Moon et al., IEEE Trans. Electron Device Lett., vol.28, pp.114-116, 2007.
- [5] I. Inoue et al., IEEE Trans. Electron Devices, vol.50, pp.43-47, 2003.
- [6] H. Han et al., Int. Image Sensor Workshop, pp.238-240, 2007.
- [7] B. Mheen et al., IEEE Trans. Electron Device Lett., vol.29, pp.347-349, 2008.
- [8] J-H. Park et al., ISSCC Dig. Tech. Papers, pp.268-269, 2009.
- [9] J. Bogaerts and B. Dierickx., Proc. SPIE vol.3965, pp.157-167, 2000.
- [10] C. Chang et al., IEEE Trans. Electron Device Lett., vol.9, pp.588-590, 1988.
- [11] L. Selmi et al., IEDM Dig. Tech. Papers, pp.333-336, 1993.
- [12] Z. A. Weinberg and A. Hartstein, Solid State Commun., vol.20, pp.179-182, 1976.
- [13] A. M. Goodman, Phys. Rev., vol.152, pp.780-784, 1966.
- [14] R. Williams, Phys. Rev., vol.140, pp.569-575, 1965.

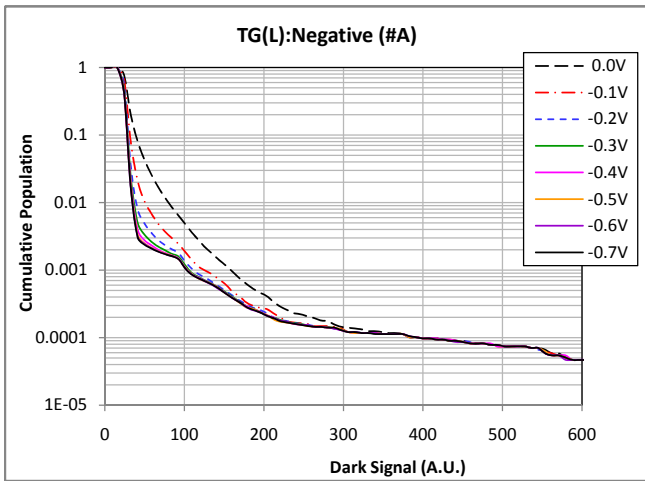


Fig. 1 Dark signal distribution of 270k pixels on negative TG biases.

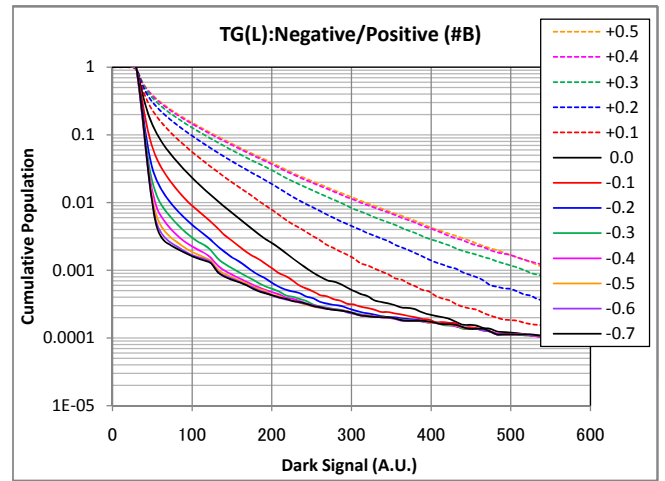


Fig. 2 Dark signal distribution of 270k pixels on positive and negative TG biases.

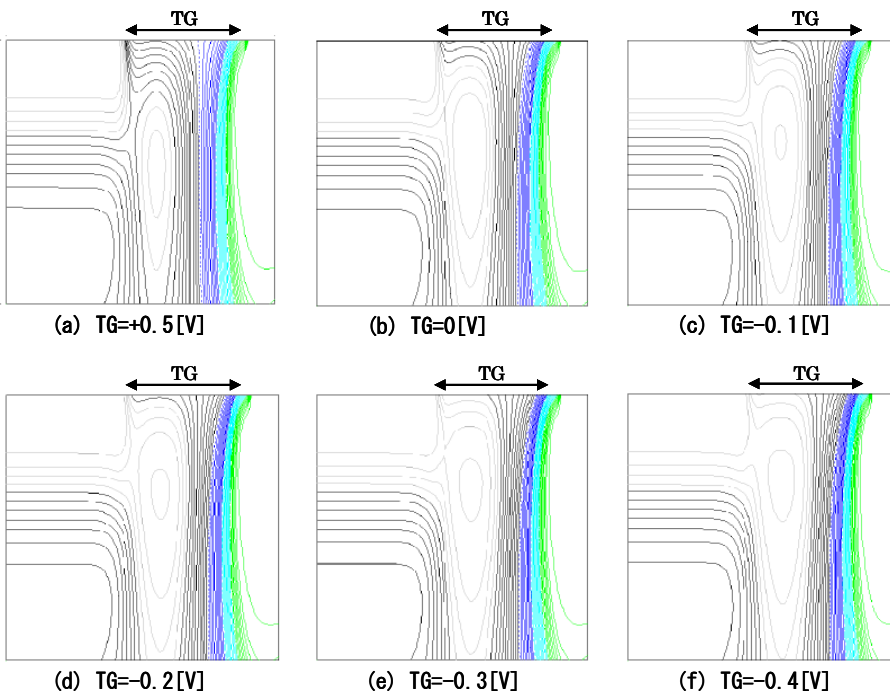


Fig. 3 Device simulations around transfer gate at various TG gate voltage.

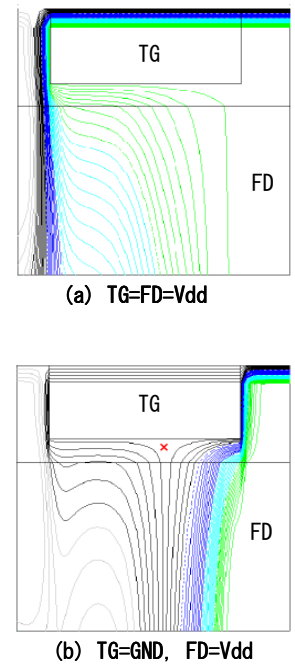


Fig. 4 Device simulations when TG is Vdd or GND.

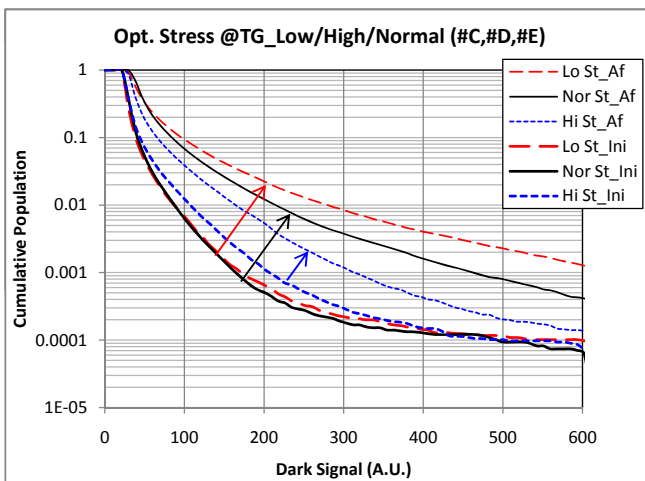


Fig. 5 Effects of optical stress for dark signal at several TG conditions.

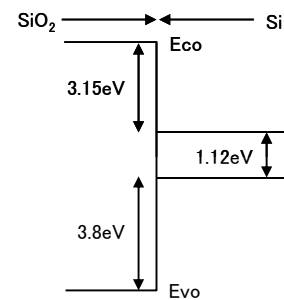


Fig. 6 Schematic energy band diagram around Si/SiO₂ interface.

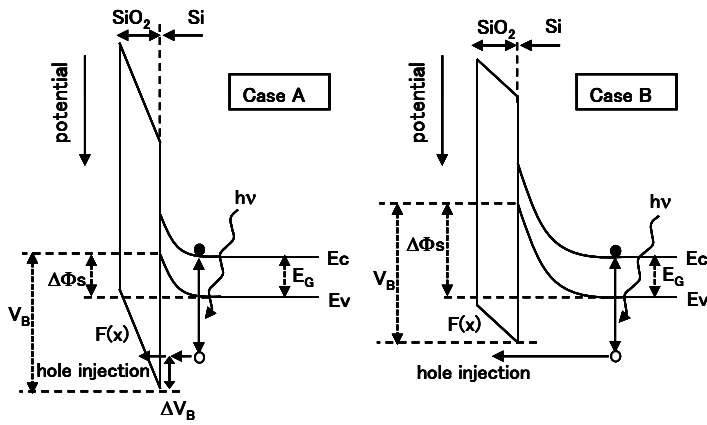


Fig. 7 Schematic illustration of hole injection.
Case A: Photon-assisted tunneling,
Case B: Photon-field-assisted emission.

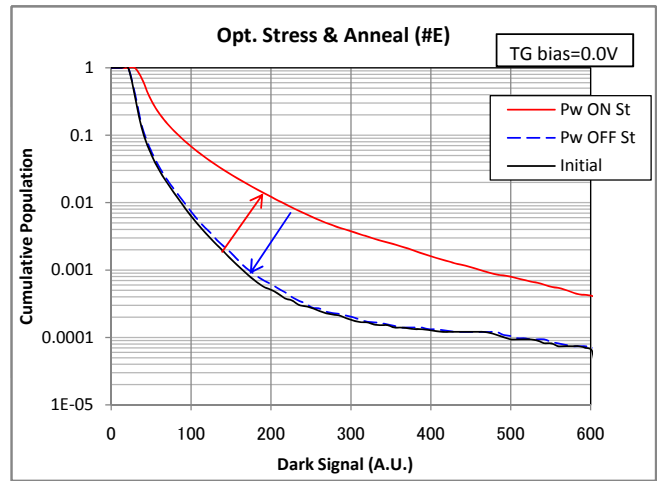


Fig. 8 Optical annealing effect on dark signal for stressed imager.

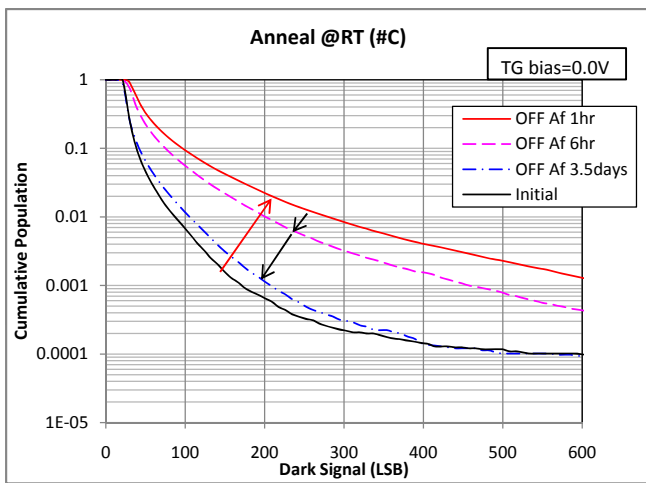


Fig. 9 Storage annealing effect for stressed imager.

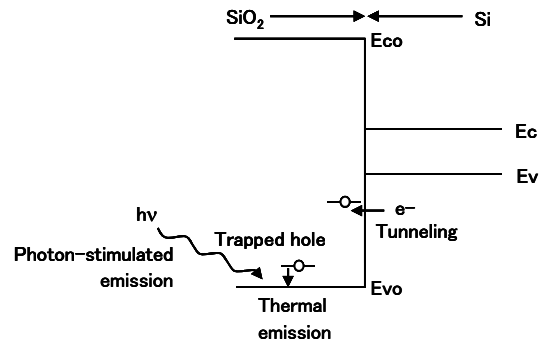


Fig. 10 Schematic illustration of two annealing mechanisms without bias.

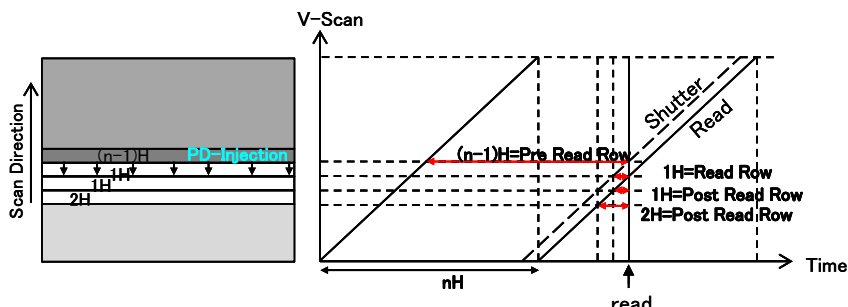
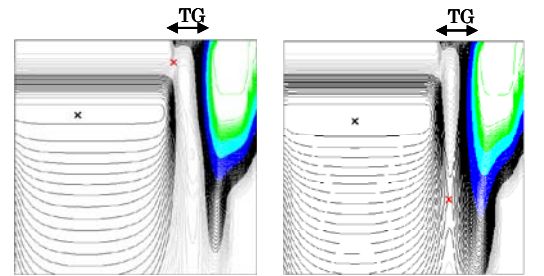


Fig. 11 Schematic diagrams in 1H shutter mode.



(a) Conventional (b) Half-side lowered conc.
Fig. 12 Device simulations around transfer gate.

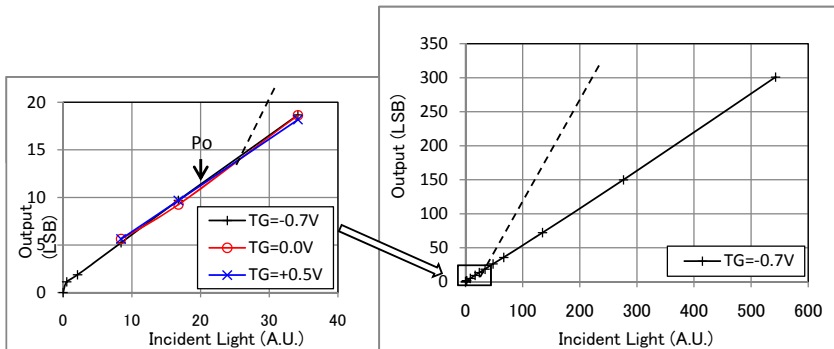


Fig. 13 Transfer curves on several bias conditions in shutter mode operation. Non-linearity like dotted line is not observed.

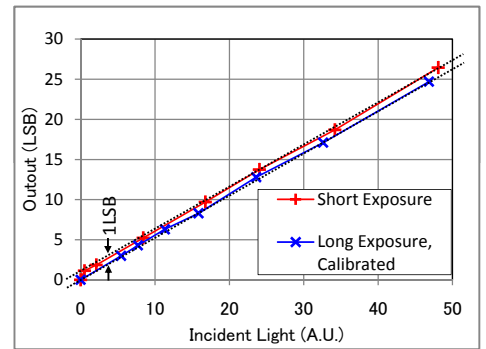


Fig. 14 Comparison between short exposure shutter mode and full frame exposure mode.